## GENERAL DESCRIPTION

The XR17D154[1] (D154) is a quad PCI Bus Universal Asynchronous Receiver and Transmitter (UART) with same package and pin-out as the Exar XR17C158, XR17D158 and XR17C154. The device is designed to meet today's 32-bit PCI Bus and high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 4 channels to speed up interrupt parsing. Each UART is independently controlled and has its own 16C550 compatible 5G register set, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO trigger levels, transmit and receive FIFO level counters, automatic hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, 8 multi-purpose inputs/outputs and a 16-bit general purpose timer/counter.

***NOTE:*** *1 Covered by U.S. Patents #5,649,122, #5,949,787*

### *APPLICATIONS*

- Universal Form Factor PCI Bus Add-in Card
- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

## FEATURES

- High Performance Quad PCI UART
- Universal PCI Bus Buffers - Auto-sense 3.3V or 5V Operation
- 32-bit PCI Bus 2.3 Target Signalling Compliance
- A Global Interrupt Source Register for all 4 UARTs
- Data Transfer in Byte, Word and Double-word
- Data Read/Write Burst Operation
- Each UART is independently controlled with:
  - 16C550 Compatible 5G Register Set
  - 64-byte Transmit and Receive FIFOs
  - Transmit and Receive FIFO Level Counters
  - Automatic RTS/CTS or DTR/DSR Flow Control
  - Automatic Xon/Xoff Software Flow Control
  - Automatic RS485 Half-duplex Control Output with Selectable Turn-around Delay
  - Infrared (IrDA 1.0) Data Encoder/Decoder
  - Programmable Data Rate with Prescaler
  - Up to 6.25 Mbps Serial Data Rate at 8X
- Eight Multi-Purpose Inputs/outputs
- General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up
- EEPROM Interface for PCI Configuration
- Same package and pin-out as the XR17D158, XR17C158 and XR17C154 (20x20x1.4mm 144-LQFP)

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

**FIGURE 1. BLOCK DIAGRAM**

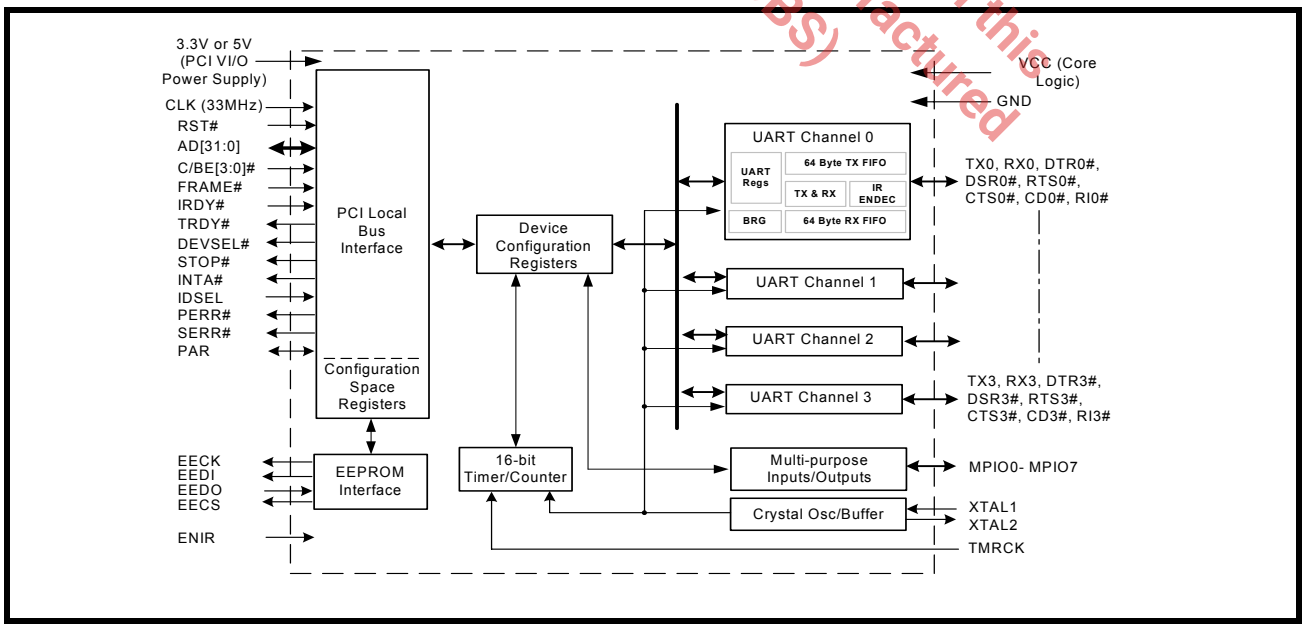
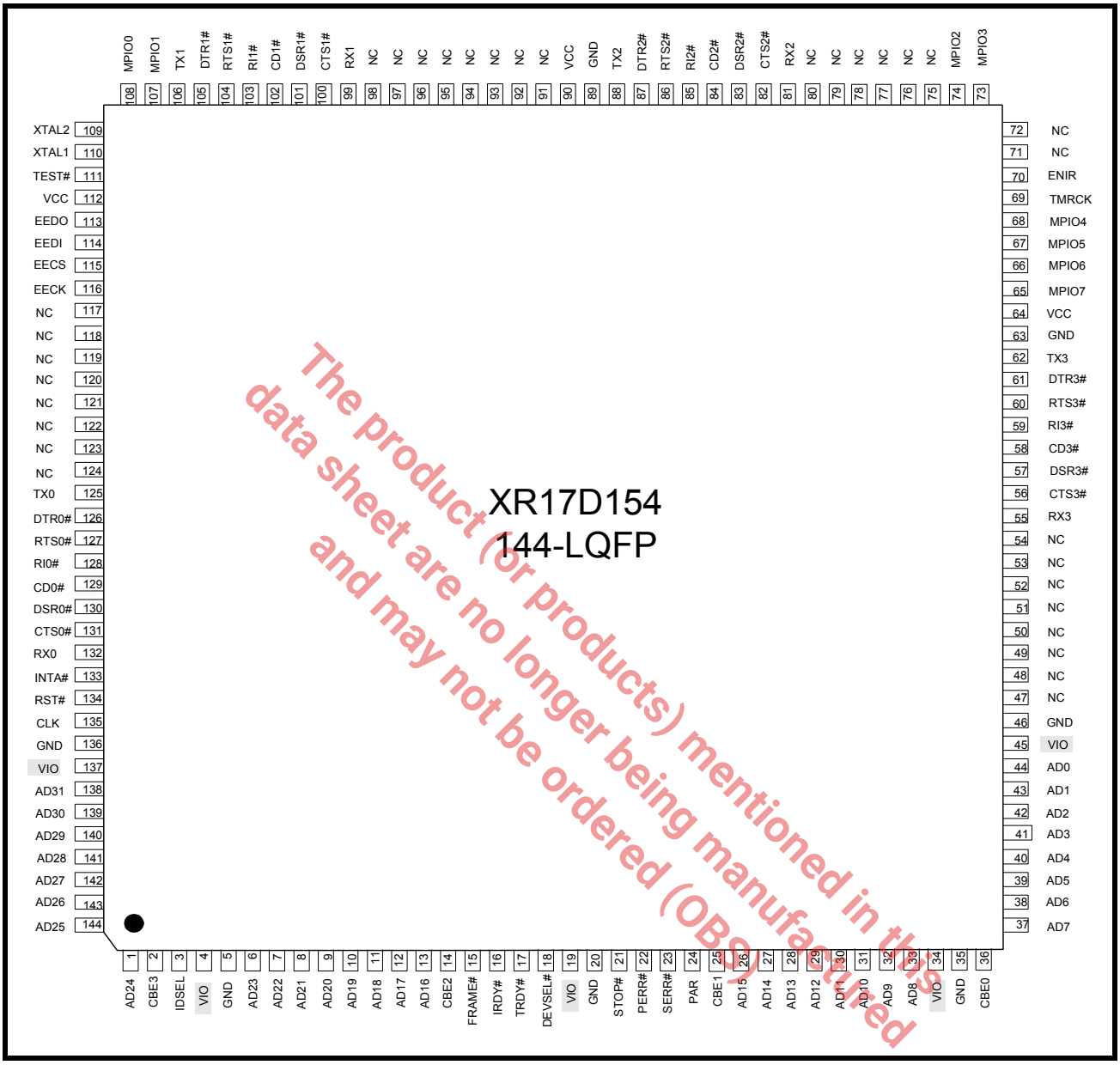


**FIGURE 2. PIN OUT OF THE DEVICE**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## *ORDERING INFORMATION*

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE | DEVICE STATUS |
|---|---|---|---|
| XR17D154CV | 144-Lead LQFP | 0°C to +70°C | Active |
| XR17D154IV | 144-Lead LQFP | -40°C to +85°C | Active |

## PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| **PCI LOCAL BUS INTERFACE** | | | |
| RST# | 134 | I | PCI Bus reset input (active low). It resets the PCI local bus configuration space registers, device configuration registers and UART channel registers to the default condition. |
| CLK | 135 | I | PCI Bus clock input of up to 33.34MHz. |
| AD31-AD25, AD24, AD23-AD16, AD15-AD8, AD7-AD0 | 138-144, 1, 6-13 26-33 37-44 | IO | Address data lines [31:0] (bidirectional). |
| FRAME# | 15 | I | Bus transaction cycle frame (active low). It indicates the beginning and duration of an access. |
| C/BE3#-C/BE0# | 2,14,25,36 | I | Bus Command/Byte Enable [3:0] (active low). This line is multiplexed for bus Command during the address phase and Byte Enable during the data phase. |
| IRDY# | 16 | I | Initiator Ready (active low). During a write, it indicates valid data is present on data bus. During a read, it indicates the master is ready to accept data. |
| TRDY# | 17 | O | Target Ready (active low). |
| STOP# | 21 | O | Target request to stop current transaction (active low). 5 |
| IDSEL | 3 | I | Initialization device select (active high). |
| DEVSEL# | 18 | O | Device select to the XR17D154 (active low). |
| INTA# | 133 | OD | Device interrupt from XR17D154 (open drain, active low). |
| PAR | 24 | IO | Parity is even across AD[31:0] and C/BE[3:0]# (bidirectional, active high). |
| PERR# | 22 | O | Parity error indicator to host (active low). Optional in bus target application. |
| SERR# | 23 | OD | System error indicator to host (open drain, active low). Optional in bus target application. |
| **MODEM OR SERIAL I/O INTERFACE** | | | |
| TX0 | 125 | O | UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX0 | 132 | I | UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS0# | 127 | O | UART channel 0 Request to Send or general purpose output (active low). |
| CTS0# | 131 | I | UART channel 0 Clear to Send or general purpose input (active low). |
| DTR0# | 126 | O | UART channel 0 Data Terminal Ready or general purpose output (active low). |
| DSR0# | 130 | I | UART channel 0 Data Set Ready or general purpose input (active low). |
| CD0# | 129 | I | UART channel 0 Carrier Detect or general purpose input (active low). |
| RI0# | 128 | I | UART channel 0 Ring Indicator or general purpose input (active low). |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| TX1 | 106 | O | UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX1 | 99 | I | UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS1# | 104 | O | UART channel 1 Request to Send or general purpose output (active low). |
| CTS1# | 100 | I | UART channel 1 Clear to Send or general purpose input (active low). |
| DTR1# | 105 | O | UART channel 1 Data Terminal Ready or general purpose output (active low). |
| DSR1# | 101 | I | UART channel 1 Data Set Ready or general purpose input (active low). |
| CD1# | 102 | I | UART channel 1 Carrier Detect or general purpose input (active low). |
| RI1# | 103 | I | UART channel 1 Ring Indicator or general purpose input (active low). |
| TX2 | 88 | O | UART channel 2 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX2 | 81 | I | UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS2# | 86 | O | UART channel 2 Request to Send or general purpose output (active low). |
| CTS2# | 82 | I | UART channel 2 Clear to Send or general purpose input (active low). |
| DTR2# | 87 | O | UART channel 2 Data Terminal Ready or general purpose output (active low). |
| DSR2# | 83 | I | UART channel 2 Data Set Ready or general purpose input (active low). |
| CD2# | 84 | I | UART channel 2 Carrier Detect or general purpose input (active low). |
| RI2# | 85 | I | UART channel 2 Ring Indicator or general purpose input (active low). |
| TX3 | 62 | O | UART channel 3 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX3 | 55 | I | UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS3# | 60 | O | UART channel 3 Request to Send or general purpose output (active low). |
| CTS3# | 56 | I | UART channel 3 Clear to Send or general purpose input (active low).d. |
| DTR3# | 61 | O | UART channel 3 Data Terminal Ready or general purpose output (active low). |
| DSR3# | 57 | I | UART channel 3 Data Set Ready or general purpose input (active low). |
| CD3# | 58 | I | UART channel 3 Carrier Detect or general purpose input (active low). |
| RI3# | 59 | I | UART channel 3 Ring Indicator or general purpose input (active low). |
| **ANCILLARY SIGNALS** | | | |
| MPIO0 | 108 | I/O | Multi-purpose input/output 0. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT |

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| MPIO1 | 107 | I/O | Multi-purpose input/output 1. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| MPIO2 | 74 | I/O | Multi-purpose input/output 2. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| MPIO3 | 73 | I/O | Multi-purpose input/output 3. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| MPIO4 | 68 | I/O | Multi-purpose input/output 4. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| MPIO5 | 67 | I/O | Multi-purpose input/output 5. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| MPIO6 | 66 | I/O | Multi-purpose input/output 6. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| MPIO7 | 65 | I/O | Multi-purpose input/output 7. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT. |
| EECK | 116 | O | Serial clock to EEPROM. An internal clock of CLK divide by 256 is used for reading the vendor and sub-vendor ID and model number during power up or reset. However, it can be manually clocked thru the Configuration Register REGB. |
| EECS | 115 | O | Chip select to a EEPROM device like 93C46. It is manually selectable thru the Configuration Register REGB. Requires a pull-up 4.7KΩ resistor for external sensing of EEPROM during power up. See DAN112 for further details. |
| EEDI | 114 | O | Write data to EEPROM device. It is manually accessible thru the Configuration Register REGB. The D154 auto-configuration register interface logic uses the 16-bit format. |
| EEDO | 113 | I | Read data from EEPROM device. It is manually accessible thru the Configuration Register REGB. |
| XTAL1 | 110 | I | Crystal of up to 24MHz or external clock input of up to 50MHz for data rates up to 6.25Mbps at 5V and 8X sampling. See AC Characterization table. Caution: this input is not 5V tolerant at 3.3V. |
| XTAL2 | 109 | O | Crystal or buffered clock output. |
| TMRCK | 69 | I | 16-bit timer/counter external clock input. |
| ENIR | 70 | I | Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 4 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART. Software can override this pin thereafter and enable or disable it. |
| TEST# | 111 | I | Factory Test. Connect to VCC for normal operation. |
| VCC | 64, 90, 112 | PWR | 5V or 3.3V power supply for the core logic. This power supply determines the VOH level of the non-PCI bus interface outputs. Note that **VCC ≥ VIO** for normal device operation and see **Table 1** for valid combinations of VCC and VIO. **SEE"APPLICATION EXAMPLES" ON PAGE 8.** However, **VCC must equal VIO** if sleep mode is used**.** See **Sleep Mode** section on page 19**.** |

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| VIO | 4, 19, 34, 45, 137 | PWR | PCI bus I/O power supply - 3.3V or 5V, detected by the auto-sense circuitry of the XR17D154. This power supply determines the VOH level of the PCI bus interface outputs.<br>(PCI 2.3 signalling compliant at both 3.3V and 5V operation, suitable for universal form factor add-in card application.) |
| GND | 5,20,35,46,63, 89,136 | PWR | Power supply common, ground. |
| NC | 47-54, 71, 72, 75-80, 91-98, 117-124 | | No Connection. These pins are reserved and used by the octal PCI UARTs XR17C158 and XR17D158. |

***NOTE:*** *Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.*

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## FUNCTIONAL DESCRIPTION

The XR17D154 (D154) integrates the functions of 4 enhanced 16550 UARTs with the PCI Local Bus interface and a non-volatile memory interface for PCI bus's plug-and-play auto-configuration, a 16-bit timer/counter, 8 multi-purpose inputs/outputs, and an on-chip oscillator. The PCI local bus is a synchronous timing bus where all bus transactions are associated to the bus clock of up to 33 MHz. The D154 supports 32-bit wide read and write data transfer operations including data burst mode through the PCI Local Bus interface. Read and write data operations maybe in byte, word or double-word (DWORD) format. The data transfer rate in a DWORD operation is 4 times faster than the single byte operation with 8-bit ISA bus. A single 32-bit interrupt status register provides interrupts status for all 4 UARTs, timer/counter, multipurpose inputs/outputs, and a special sleep wake up indicator. There are three sets of register in the device. First, the PCI local bus configuration registers for PCI auto configuration. A set of device configuration registers for overall control, 32-bit wide transmit and receive data transfer, and monitoring of the 4 UART channels. Lastly, each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and byte wide data transfer.

Each UART has the improved fifth generation (5G) register set, 64-byte FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger level, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of 1X or 4X, and data rate up to 6.25 Mbps. The XR17D154 bus timing and drive capability meets the PCI local bus specification revision 2.3 for 3.3V and 5V at 33.34 MHz over the temperature range. The XR17D154 is available in the same thin 144-pin LQFP (20x20x1.4mm) package and pin-out as the XR17C154, XR17D158 and XR17C158 in commercial and industrial temperature ranges.

The product for product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

### PCI LOCAL BUS INTERFACE

This is the host interface and it meets the PCI Local Bus Specification revision 2.3. The PCI local bus operations are synchronous meaning each transaction is associated to the bus clock. The XR17D154 can operate with the bus clock of up to a 33.34 MHz. Data transfers operation can be formatted in 8-bit, 16-bit, 24-bit or 32-bit wide. With 32-bit data operations, it pushes the data transfer rate on the bus up to 132 MByte/sec. This increases the overall system's communication performance up to 16 times better than the 8-bit ISA bus. See PCI local bus specification revision 2.3 for bus operation details.

### PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

A set of PCI local bus configuration space register is provided. These registers provide the PCI local bus operating system with the card's vendor ID, device ID, sub-vendor ID, product model number, and resources and capabilities. The PCI local bus operating system collects this data from all the cards on the bus during the auto configuration phase that follows immediately after a power up or system reset/reboot. After it has sorted out all devices on the bus, it defines and download the operating conditions to the cards. One of the definitions is the base address loaded into the Base Address Register (BAR) where the card will be operating in the PCI local bus memory space.

### EEPROM INTERFACE

An external 93C46 EEPROM is only used to store the vendor's ID and model number, and the sub-vendor's ID and product model number. This information is only used with the plug-and-play auto configuration of the PCI local bus. These data provide automatic hardware installation onto the PCI bus. The EEPROM interface consists of 4 signals, EEDI, EEDO, EECS, and EECK. The EEPROM is not needed when auto configuration is not required in the application. However, If your design requires non-volatile memory for other purpose. It is possible to store and retrieve data on the EEPROM through a special PCI device configuration register. See application note DAN112 for its programming details.

## 1.0 APPLICATION EXAMPLES

The XR17D154 is designed to operate with VCC (voltage to the UART Core Logic) greater than or equal to VIO. See Table 1 below for valid combintions of VCC and VIO that can be used with the device..

**TABLE 1: VALID COMBINATIONS OF VCC AND VIO SUPPLY VOLTAGES**

| VCC | VIO | |
|---|---|---|
| 5.0V | 5.0V | Valid |
| 5.0V | 3.3V | Valid |
| 3.3V | 5.0V | ***Invalid*** |
| 3.3V | 3.3V | Valid |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

For a universal add-in card, it is usually unknown whether it will be plugged into a 3.3V or 5V PCI slot, therefore VCC must be 5V to guarantee proper functionality in any PCI slot as shown in Figure 3. In an embedded system, the designer can choose to use a 3.3V or 5V power supply for the UART core voltage. Of course, the core voltage can be 3.3V only when the VIO is 3.3V. In Figure 4, examples 1-3 show valid applications of the XR17D154 in an embedded system.

**FIGURE 3. TYPICAL APPLICATION FOR A UNIVERSAL ADD-IN CARD**

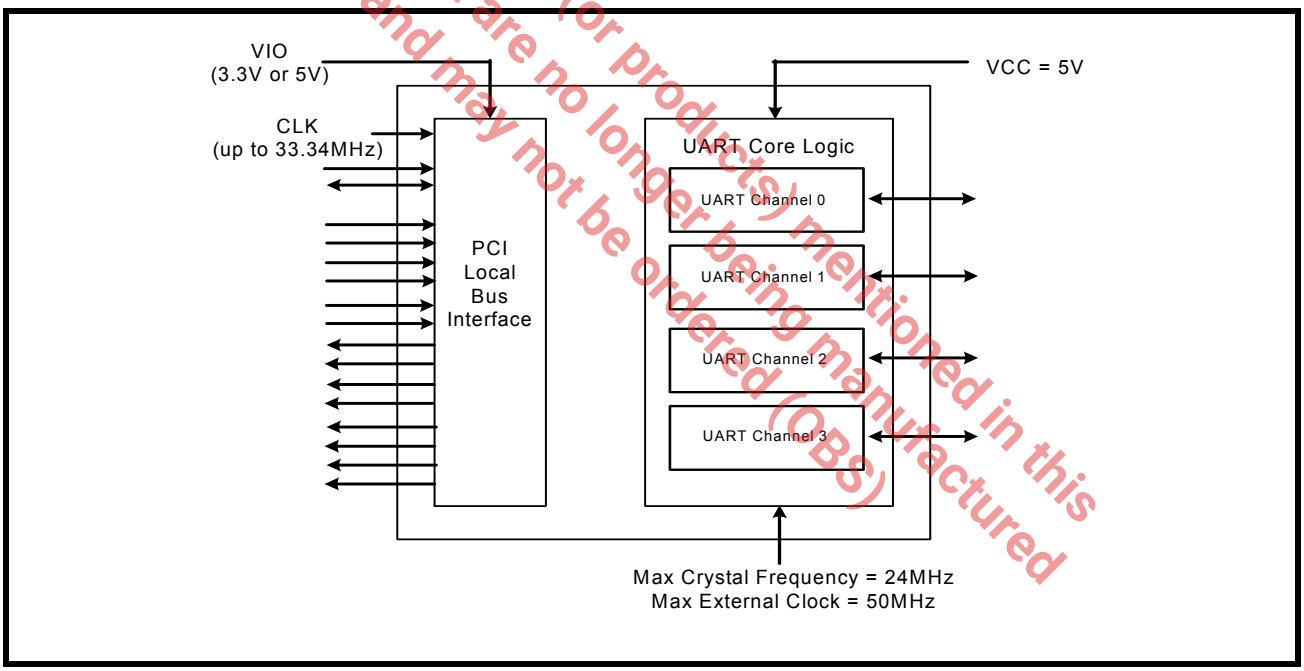
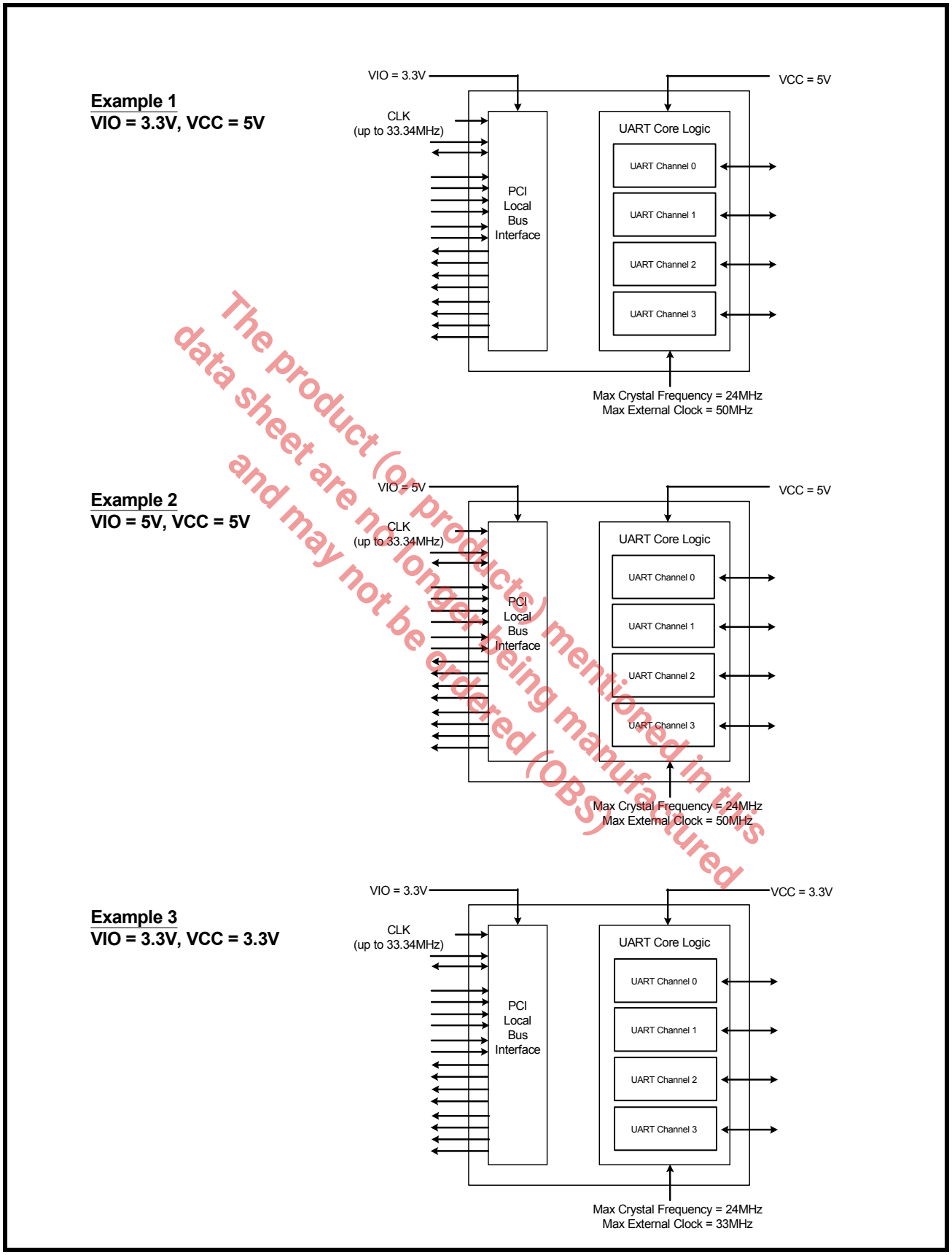


FIGURE 4. TYPICAL APPLICATIONS IN AN EMBEDDED SYSTEM



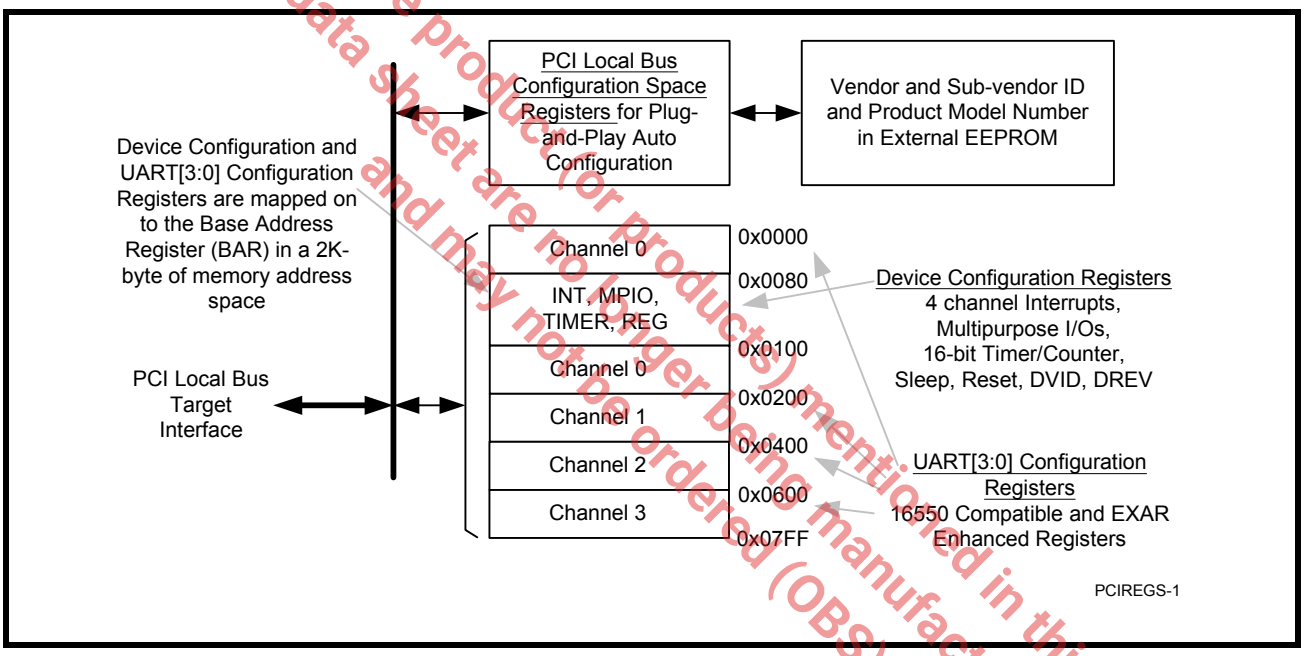

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## 2.0 XR17D154 REGISTERS

The XR17D154 UART has three different sets of registers as shown in Figure 5. The PCI local bus configuration space registers are for plug-and-play auto-configuration when connecting the device to the PCI bus. This auto-configuration feature makes installation very easy into a PCI system and it is part of the PCI local bus specification. The second register set is the device configuration registers that are accessible directly from the PCI bus for programming general operating conditions of the device and monitoring the status of various functions. These registers are mapped into 2K of the PCI bus memory address space. These functions include all 4 channel UART's interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode, soft-reset, and device identification and revision. And lastly, each UART channel has its own set of 5G internal UART configuration registers for its own operation control and status reporting. All 4 sets of channel registers are embedded inside the device configuration registers space, which provides faster access. The following paragraphs describe all 3 sets of registers in detail.

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**FIGURE 5. THE XR17D154 REGISTER SETS**




### 2.1 PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

The PCI local bus configuration space registers are responsible for setting up the device's operating environment in the PCI local bus. The pre-defined operating parameters of the device are read by the PCI bus plug-and-play auto-configuration manager in the operating system. After the PCI bus has collected all data from every device/card on the bus, it defines and downloads the memory mapping information to each device/card about their individual operation memory address location and conditions. The operating memory mapped address location is downloaded into the Base Address Register (BAR) register, 0x10. The plug-and-play auto configuration feature is only available when an external 93C46 EEPROM is used. The EEPROM contains the device vendor and sub-vendor data required by the auto-configuration setup.

**TABLE 2: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS**

| ADDRESS | BITS | TYPE | DESCRIPTION | RESET VALUE (HEX) |
|---|---|---|---|---|
| 0x00 | 31:16 | RWR[1] | Device ID (Exar device ID number or from EEPROM) | 0x0154 |
| | 15:0 | RWR[1] | Vendor ID (Exar ID or from EEPROM) specified by PCISIG | 0x13A8 |
| 0x04 | 31:28 | RO | Status bits (error reporting bits) | 0000 |
| | 27 | R-Reset | Target Abort. Set whenever D154 terminates with a target abort. | 0 |
| | 26:25 | RO | DEVSEL# timing. | 00 |
| | 24 | RO | Unimplemented bus master error reporting bit | 0 |
| | 23 | RO | Fast back to back transactions are supported | 1 |
| | 22:16 | RO | Reserved Status bits | 000 0000 |
| | 15:9,7, 5,4,3,2 | RO | Command bits (reserved) | 0x0000 |
| | 8 | WO | SERR# driver enable. Logic 1=enable driver and 0=disable driver | 0 |
| | 6 | WO | Parity error enable. Logic 1=respond to parity error and 0=ignore | 0 |
| | 1 | RWR | Command controls a device's response to mem space accesses: 0=disable mem space accesses, 1=enable mem space accesses | 0 |
| | 0 | RO | Command controls a device's response to I/O space accesses: 0 = disable I/O space accesses 1 = enable I/O space accesses | 0 |
| 0x08 | 31:8 | RO | Class Code (Simple 550 Communication Controller). | 0x070002 |
| | 7:0 | RO | Revision ID (Exar device revision number) | Current Rev. value |
| 0x0C | 31:24 | RO | BIST (Built-in Self Test) | 0x00 |
| | 23:16 | RO | Header Type (a single function device with one BAR) | 0x00 |
| | 15:8 | RO | Unimplemented Latency Timer (needed only for bus master) | 0x00 |
| | 7:0 | RO | Unimplemented Cache Line Size | 0x00 |
| 0x10 | 31:11 | RW | Memory Base Address Register (BAR) | 0x00 |
| | 10:0 | RO | Claims a 2K address space for the memory mapped UARTs | 0xX000 |
| 0x14 | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x18h | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x1C | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x20 | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x24 | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x28 | 31:0 | RO | Reserved | 0x00000000 |
| 0x2C | 31:16 | RWR[1] | Subsystem ID (write from external EEPROM by customer) | 0x0000 |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OPS)

**TABLE 2: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS**

| ADDRESS | BITS | TYPE | DESCRIPTION | RESET VALUE (HEX) |
|---|---|---|---|---|
| | 15:0 | RWR[1] | Subsystem Vendor ID (write from external EEPROM by customer) | 0x0000 |
| 0x30 | 31:0 | RO | Expansion ROM Base Address (Unimplemented) | 0x00000000 |
| 0x34 | 31:0 | RO | Reserved (returns zeros) | 0x00000000 |
| 0x38 | 31:0 | RO | Reserved (returns zeros) | 0x00000000 |
| 0x3C | 31:24 | RO | Unimplemented MAXLAT | 0x00 |
| | 23:16 | RO | Unimplemented MINGNT | 0x00 |
| | 15:8 | RO | Interrupt Pin, use INTA#. | 0x01 |
| | 7:0 | RWR | Interrupt Line. | 0xXX |

*NOTE: RWR[1]=Read/Write from external EEPROM. RWR=Read/Write from AD[31:0]. RO= Read Only. WO=Write Only.*

### 2.2 Device configuration Register Set

The device configuration registers and a special way to access each of the UART's transmit and receive data FIFOs are accessible directly from the PCI data bus. This provides easy programming of general operating parameters to the D154 UART and for monitoring the status of various functions. The registers occupy 2K of PCI bus memory address space. These addresses are offset onto the basic memory address, a value loaded into the Memory Base Address Register (BAR) in the PCI local bus configuration register set. These registers control or report on all 4 channel UARTs functions that include interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode control, soft-reset control, and device identification and revision, and others.

The registers set is mapped into 4 address blocks where each UART channel occupies 512 bytes memory space for its own 16550 compatible configuration registers. The device configuration and control registers are embedded inside the UART channel zero's address space between 0x0080 to 0x0093. All these registers can be accessed in 8, 16, 24 or 32 bit width depending on the starting address given by the host at beginning of the bus cycle. Transmit and receive data may be loaded or unloaded in 8, 16, 24 or 32 bit format to the register's address. Every time a read or write operation is made to the transmit or receive register, its FIFO data pointer is automatically bumped to the next sequential data location either in byte, word or dword. One special case applies to the receive data unloading when reading the receive data together with its LSR register content. The host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

**TABLE 3: XR17D154 DEVICE CONFIGURATION REGISTERS**

| OFFSET ADDRESS | MEMORY SPACE | READ/WRITE | DATA WIDTH | COMMENT |
|---|---|---|---|---|
| 0x000 - 0x00F | UART channel 0 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x010 - 0x07F | Reserved | | | |
| 0x080 - 0x093 | DEVICE CONFIG. REGISTERS | (Table 4) | 8/16/24/32 | |
| 0x094 - 0x0FF | Reserved | Read/Write | | |
| 0x100 - 0x13F | UART 0 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x100 - 0x13F | UART 0 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x140 - 0x17F | Reserved | | | |
| 0x180 - 0x1FF | UART 0 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |
| | | | | |
| 0x200 - 0x20F | UART channel 1 Regs | (Table 12 & Table 13) | 8/16//24/32 | First 8 regs are 16550 compatible |
| 0x210 - 0x2FF | Reserved | Read/Write | | |
| 0x300 - 0x33F | UART 1 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x300 - 0x33F | UART 1 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x340 - 0x37F | Reserved | | | |
| 0x380 - 0x3FF | UART 1 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |
| | | | | |
| 0x400 - 0x40F | UART channel 2 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x410 - 0x4FF | Reserved | Read/Write | | |
| 0x500 - 0x53F | UART 2 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x500 - 0x53F | UART 2 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x540 - 0x57F | Reserved | | | |
| 0x580 - 0x5FF | UART 2 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |
| | | | | |
| 0x600 - 0x60F | UART channel 3 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x610 - 0x6FF | Reserved | Read/Write | | |
| 0x700 - 0x73F | UART 3 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x700 - 0x73F | UART 3 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x740 - 0x77F | Reserved | | | |
| 0x780 - 0x7FF | UART 3 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 4: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT**

| ADDRESS [A7:A0] | REGISTER | READ/WRITE COMMENT | RESET STATE |
|---|---|---|---|
| Ox080 | INT0 [7:0] | Read-only Interrupt [3:0], Reserved [7:4] | Bits 7-0 = 0x00 |
| Ox081 | INT1 [15:8] | Read-only | Bits 7-0 = 0x00 |
| Ox082 | INT2 [23:16] | Read-only [3:0], Reserved [7:4] | Bits 7-0 = 0x00 |
| Ox083 | INT3 [31:24] | Reserved | Bits 7-0 = 0x00 |
| | | | |
| Ox084 | TIMERCNTL | Read/Write Timer Control | Bits 7-0 = 0x00 |
| Ox085 | TIMER | Reserved | Bits 7-0 = 0x00 |
| Ox086 | TIMERLSB | Read/Write Timer LSB | Bits 7-0 = 0x00 |
| Ox087 | TIMERMSB | Read/Write Timer MSB | Bits 7-0 = 0x00 |
| | | | |
| Ox088 | 8XMODE | Read/Write | Bits 7-0 = 0x00 |
| Ox089 | REGA | Reserved | Bits 7-0 = 0x00 |
| Ox08A | RESET | Write-only Self clear bits after executing Reset [3:0] | Bits 7-0 = 0x00 |
| Ox08B | SLEEP | Read/Write Sleep mode [3:0] | Bits 7-0 = 0x00 |
| | | | |
| Ox08C | DREV | Read-only Device revision | Bits 7-0 = 0x04 |
| Ox08D | DVID | Read-only Device identification | Bits 7-0 = 0x24 |
| Ox08E | REGB | Read/Write | Bits 7-0 = 0x00 |
| Ox08F | MPIOINT | Read/Write MPIO interrupt mask | Bits 7-0 = 0x00 |
| | | | |
| Ox090 | MPIOLVL | Read/Write MPIO level control | Bits 7-0 = 0x00 |
| Ox091 | MPIO3T | Read/Write MPIO output control | Bits 7-0 = 0x00 |
| Ox092 | MPIOINV | Read/Write MPIO input polarity select | Bits 7-0 = 0x00 |
| Ox093 | MPIOSEL | Read/Write MPIO select | Bits 7-0 = 0xFF |

The product(or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 5: DEVICE CONFIGURATION REGISTERS SHOWN IN DWORD ALIGNMENT**

| ADDRESS | REGISTER | BYTE 3 [31:24] | BYTE 2 [23:16] | BYTE 1 [15:8] | BYTE 0 [7:0] |
|---|---|---|---|---|---|
| 0x080-083 | INTERRUPT (read-only) | INT3 | INT2 | INT1 | INT0 |
| 0x084-087 | TIMER (read/write) | TIMERMSB | TIMERLSB | TIMER (reserved) | TIMERCNTL |
| 0x088-08B | ANCILLARY1 (read/write) | SLEEP | RESET | REGA (reserved) | 8XMODE |
| 0x08C-08F | ANCILLARY2 (read-only) | MPIOINT | REGB | DVID | DREV |
| 0x090-093 | MPIO (read/write) | MPIOSEL | MPIOINV | MPIO3T | MPIOLVL |

### 2.2.1 The Interrupt Status Register

The XR17D154 has a 32-bit wide register [INT0, INT1, INT2 and INT3] to provide interrupt information and supports two interrupt schemes. The first scheme uses bits 0 to 3 of an 8-bit indicator (INT0) representing channels 0 to 3 of the XR17D154, respectively. This permits the interrupt routine to quickly vector and serve that UART channel and determine the source(s) in each individual routines. INT0 bit-0 represents the interrupt status for UART channel 0 when its transmitter, receiver, line status, or modem port status requires service. Other bits in the INT0 register provide indication for the other channels with bit-3 representing UART channel 4 respectively, bits 4 to 7 are reserved and remain at logic zero.

The second scheme provides detail about the source of the interrupts for each UART channel. All the interrupts are encoded into a 3-bit code. This 3-bit code represents 7 interrupts corresponding to individual UART's transmitter, receiver, line status, modem port status. INT1 and INT2 registers provide the 12-bit interrupt status for all 4 channels. Bits 8, 9 and 10 representing channel 0 and bits 17,18 and 19 representing channel 3 respectively. Bits 20 to 31 are reserved and remain at logic zero. All 4 channel interrupts status are available with a single DWORD read operation. This feature allows the host quickly vectors and serves the interrupts, reducing service interval, hence, reduce host bandwidth requirement. Figure 6 shows the 4-byte interrupt register and its make up.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**GLOBAL INTERRUPT REGISTER (DWORD) - [default 0x00-00-00-00]**

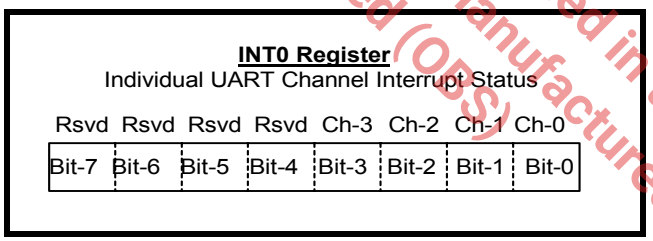
| INT3 [31:24] | INT2 [23:16] | INT1 [15:8] | INT0 [7:0] |
|---|---|---|---|

A special interrupt condition is generated by the 154 when it wakes up from sleep mode. This special interrupt is cleared by reading the INT0 register. If there are not any other interrupts pending, the value read from INT0 would be 0x00.

**INT0 [7:0] Channel Interrupt Indicator**

Each bit gives an indication of the channel that has requested for service. Bit-0 represents channel 0 and bit-3 indicates channel 3. Logic 1 indicates that a channel has called for service. Bits 4 to 7 are reserved and remain at logic 0 The interrupt bit clears after reading the appropriate register of the interrupting channel register, see Interrupt Clearing section.

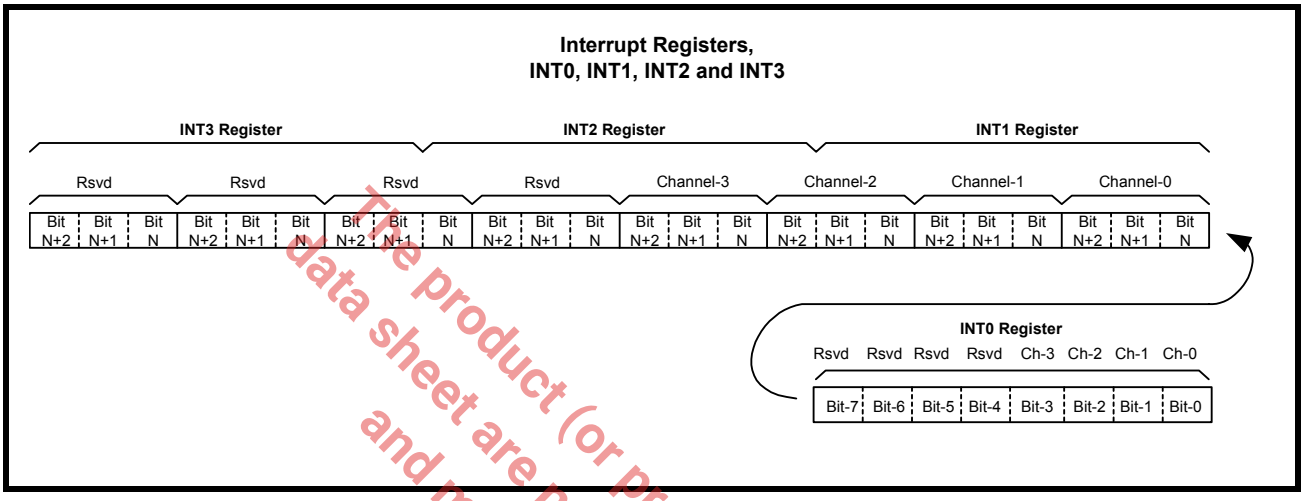
**INT0 register provides status for each channel**



### Registers INT3, INT2 and INT1 [32:8]

Twenty four bit encoded interrupt indicator. Each channel's interrupt is encoded into 3 bits for receive, transmit, and status. Bit [10:8] represent channel 0 and go up to channel 3 with bits [19:17]. The 3 bit encoding and their priority order are shown below in **Table 6**. The Timer and MPIO interrupts are for the device and therefore they exist within channel 0 space (bits [10:8]) only.

**FIGURE 6. THE GLOBAL INTERRUPT REGISTER, INT0, INT1, INT2 AND INT3**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 6: UART CHANNEL [3:0] INTERRUPT SOURCE ENCODING**

| PRIORITY | BIT[N+2] | BIT[N+1] | BIT[N] | INTERRUPT SOURCE(S) |
|---|---|---|---|---|
| x | 0 | 0 | 0 | None |
| 1 | 0 | 0 | 1 | RXRDY and RX Line Status (logic OR of LSR[4:1]) |
| 2 | 0 | 1 | 0 | RXRDY Time-out |
| 3 | 0 | 1 | 1 | TXRDY, THR or TSR (auto RS485 mode) empty |
| 4 | 1 | 0 | 0 | MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon det. or special char. detected |
| 5 | 1 | 0 | 1 | Reserved. |
| 6 | 1 | 1 | 0 | MPIO pin(s). Available only within channel 0, reserved in other channels. |
| 7 | 1 | 1 | 1 | TIMER Time-out. Available only within channel 0, reserved in other channels. |

**TABLE 7: UART CHANNEL [3:0] INTERRUPT CLEARING:**

| |
|---|
| RXRDY is cleared by reading data in the RX FIFO until it falls below the trigger level. |
| RXRDY Time-out is cleared by reading data until the RX FIFO is empty. |
| RX Line Status interrupt clears after reading the LSR register. |
| TXRDY interrupt clears after reading ISR register that is in the UART channel register set. |
| Modem Status Register interrupt clears after reading MSR register that is in the UART channel register set. |
| RTS/CTS or DTR/DSR delta interrupt clears after reading MSR register that is in the UART channel register set. |
| Xoff/Xon interrupt clears after reading the ISR register that is in the UART channel register set. |
| Special character detect interrupt is cleared by a read to ISR or after the next character is received. |
| TIMER Time-out interrupt clears after reading the TIMERCNTL register that is in the Device Configuration register set. |
| MPIO interrupt clears after reading the MPIOLVL register that is in the Device Configuration register set. |

### 2.2.2 General Purpose 16-bit Timer/Counter [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0xXX-XX-00-00)

A 16-bit down-count timer for general purpose timer or counter. Its clock source may be selected from internal crystal oscillator or externally on pin TMRCK. The timer can be set to be a single-shot for a one-time event or re-triggerable for continue interval. An interrupt may be generated in the INT Register when the timer times out. It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. These registers provide start/stop and re-triggerable or one-shot operation. The time-out output of the Timer can be set to generate an interrupt for system or event alarm.

**FIGURE 7. TIMER/COUNTER CIRCUIT.**

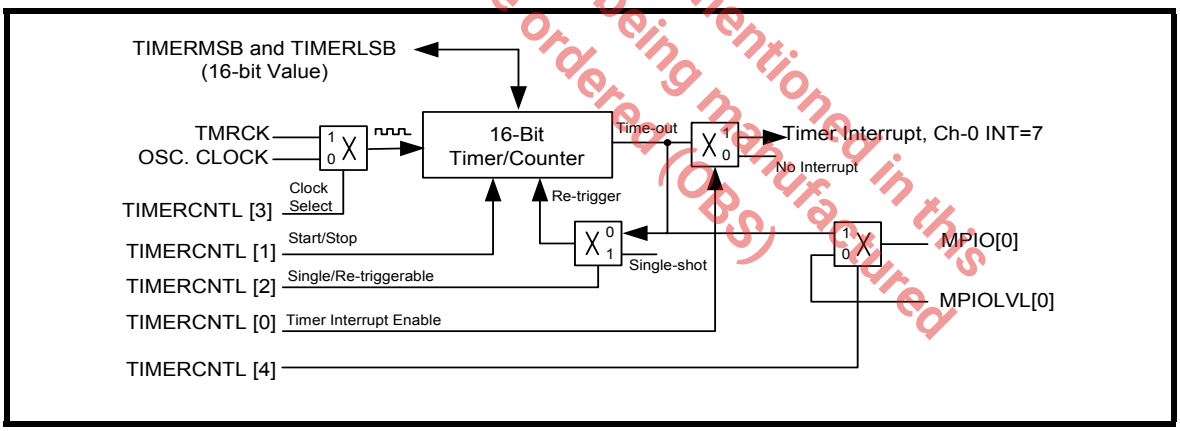



**TABLE 8: TIMER CONTROL REGISTERS**

| | |
|---|---|
| TIMERCNTL [0] | Logic zero (default) disables Timer-Counter interrupt and logic one enables the interrupt, reading the TIMERCNTL clears the interrupt. |
| TIMERCNLT [1] | Logic zero (default) stops/pauses the timer and logic one starts/re-starts the timer/counter. |
| TIMERCNTL [2] | Logic zero (default) selects re-trigger timer function and logic one selects one-shot (timer function. |
| TIMERCNTL [3] | Logic zero (default) selects internal and logic one selects external clock to the timer/counter. |
| TIMERCNTL [4] | Routes the Timer-Counter interrupt to MPIO[0] if MPIOSEL[0]=0 for external event control. |
| TIMERCNTL [7:5] | Reserved (defaults to zero) |

The product (of products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**TIMERCNTL Register**

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | MPIO[0] Control | Clock Select | Single/ Re-trigger | Start/ Stop | INT Enable |

**TIMER [15:8] - Reserved**

**TIMERMSB [31:24] and TIMERLSB [23:16]**

TIMERMSB and TIMERLSB form a 16-bit value. The least-significant bit of the timer is being bit [0] of the TIMERLSB with most-significant-bit being bit [7] in TIMERMSB. Notice that these registers do not hold the current counter value when read. Reading the TIMERCNTL register will clear its interrupt. Default value is zero (timer disabled) upon powerup and reset.

16-Bit Timer/Counter Programmable Registers

**TIMERMSB Register**

| Bit-15 | Bit-14 | Bit-13 | Bit-12 | Bit-11 | Bit-10 | Bit-9 | Bit-8 |
|---|---|---|---|---|---|---|---|

**TIMERLSB Register**

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be offered (OBS)

### 2.2.3 8XMODE [7:0] - (default 0x00)

Each bit selects 8X or 16X sampling rate for that UART channel, bit-0 is channel 0. Logic 0 (default) selects normal 16X sampling with logic one selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X.

**8XMODE Register**
Individual UART Channel 8X Clock Mode Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

### 2.2.4 REGA [15:8] Reserved

### 2.2.5 RESET [23:16] - (default 0x00)

The 8-bit Reset register [RESET] provides the software with the ability to reset the UART(s) when there is a need. Each bit is self-resetting after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see **Table 20** for details. Bit-0 =1 resets UART channel 0 with bit-3=1 resets channel 3..

**RESET Register**
Individual UART Channel Reset Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

### 2.2.6 SLEEP [31:24] - (default 0x00)

Each UART can be separately enabled to enter Sleep mode through the Sleep register. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. All of these conditions must be satisfied for the D154 to enter sleep mode:

- no interrupts pending (INT0 = 0x00)
- divisor is a non-zero value for all channels (ie. DLL = 0x1)
- sleep mode is enabled (SLEEP = 0x0F)
- modem inputs for all channels are not toggling (MSR bits 0-3 = 0)
- RX input pins for all channels are idling HIGH

The D154 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The D154 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the D154 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the D154 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The D154 will stay in the sleep mode of operation until it is disabled by setting Sleep = 0x00. In this case, the quad UART is awaken by any of the UART channel from a receive data byte or a change on the serial port. The UART is ready after 32 crystal clocks to ensure full functionality. Also, a special interrupt is generated with an indication of no pending interrupt. Reading INT0 will clear this special interrupt. Logic 0 (default) is disable and logic 1 is enable to sleep mode.

**Important**: The XR17D154 is a versatile device designed to operate with different VCC (core power supply) and VIO(PCI bus I/O power supply). However, the VCC and VIO must be equal (VCC = VIO) for the sleep mode to reduce power consumption. Any difference in these voltages will result in high currents, when placed in sleep mode. If sleep mode is used, it is recommended that both VCC and VIO be powered by the PCI bus VIO power pins. If sleep mode is not used, there is no concern about high currents whether VCC = VIO or VCC > VIO. In any case, VCC should never be less than VIO.

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**SLEEP Register**
Individual UART Channel Sleep Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

### 2.2.7 Device Identification and Revision

There are two internal registers that provide device identification and revision, DVID and DREV registers. The 8-bit content in the DVID register provides device identification. A return value of 0x24 from this register indicates the device is an XR17D154 or an XR17C154. The DREV register returns an 8-bit value of 0x01 for revision A with 0x02 equals to revision B and so forth. This information is very useful to the software driver for identifying which device it is communicating with and to keep up with revision changes.

**DVID [15:8]**

Device identification for the type of UART. The upper nibble indicates it is a XR17xxxx series with lower nibble indicating the number of channels.

Examples:

XR17D158 or XR17C158 = 0x28

XR17D154 or XR17C154 = 0x24

XR17D152 or XR17C152 = 0x22

**DREV [7:0]**

Revision number of the XR17D154. A 0x01 represents "revision-A" with 0x02 for rev-B and so forth.

**REGB [23:16] - (default 0x00)**

REGB register provides a control for simultaneous write to all 4 UARTs configuration register or individually. This is very useful for device initialization in the power up and reset routines. Also, the register provides a facility to interface to the non-volatile memory device such as a 93C46 EEPROM. In embedded applications, the user can use this facility to store proprietary data.

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 2.2.8 REGB Register

| | |
|---|---|
| REGB[16] (Read/Write) | Logic 0 (default) write to each UART configuration registers individually. |
| | Logic 1 enables simultaneous write to all 4 UARTs configuration register. |
| REGB[19:17] | Reserved |
| REGB[20] (Write-Only) | Control the EECK, clock, output (pin 116) on the EEPROM interface. |
| REGB[21] (Write-Only) | Control the EECS, chips select, output (pin 115) to the EEPROM device. |
| REGB[22] (Write-Only) | EEDI (pin 114) data input. Write data to the EEPROM device. |
| REGB[23] (Read-Only) | EEDO (pin 113) data output. Read data from the EEPROM device. |

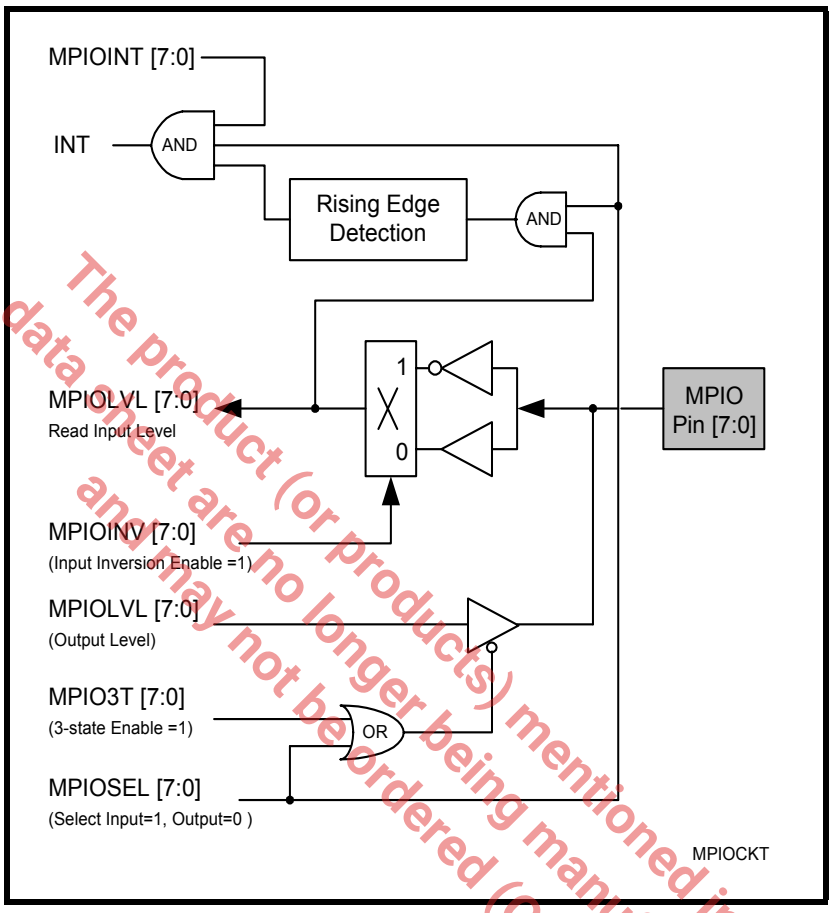
### 2.2.9 Multi-Purpose Inputs and Outputs

The D154 provides 8 multi-purpose inputs/outputs [MPIO7:0] for general use. Each pin can be programmed to be an input or output function. The input logic state can be set for normal or inverted level, and optionally set to generate an interrupt. The outputs can be set to be normal logic 1 or 0 state, or tri-state. Their functions and definitions are programmed through 5 registers: MPIOINT, MPIOLVL, MPIO3T, MPIOINV and MPIOSEL. If all 8 pins are set for inputs, all 8 interrupts would be OR'ed together. The Or'ed interrupt is reported in the channel 0 UART interrupt status, see Interrupt Status Register. The pins may also be programmed to be outputs and to the tri-state condition for signal sharing.

### 2.2.10 MPIO REGISTER

Bit 7 represents MPIO7 pin and bit 0 represents MPIO0 pin. There are 5 registers that select, control and monitor the 8 multipurpose inputs and outputs pins. Figure 8 shows the internal circuitry.

**FIGURE 8. MULTIPURPOSE INPUT/OUTPUT INTERNAL CIRCUIT**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

**MPIOINT [7:0] - (default 0x00)**

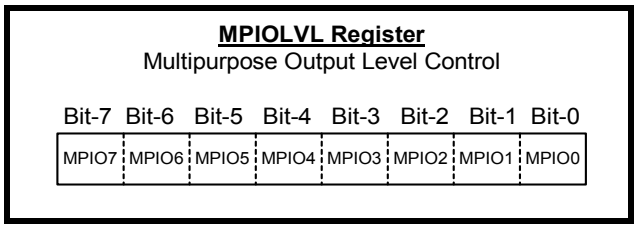
Enable multipurpose input pin interrupt. If the pin is selected by MPIOSEL as input then bit-0 enables input pin 0 for interrupt, and bit-7 enables input pin 7. No interrupt is enable if the pin is selected to be an output. The interrupt is edge sensing and determined by MPIOINV and MPIOLVL registers. The MPIO interrupt clears after a read to register MPIOLVL. The combination of MPIOLVL and MPIOINV determines the interrupt being active low or active high, it's level trigger. Logic 0 (default) disables the pin's interrupt and logic 1 enables it.

**MPIOINT Register**
Multipurpose Input/Output Interrupt Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| MPIO7 | MPIO6 | MPIO5 | MPIO4 | MPIO3 | MPIO2 | MPIO1 | MPIO0 |

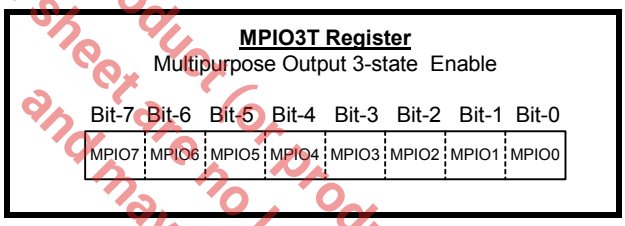
**MPIOLVL [7:0] - (default 0x00)**

Output pin level control and input level status. The status of the input pin(s) is read on this register and output pins are controlled on this register. A logic 0 (default) sets the output to low and a logic 1 sets the output pin to high. The MPIO interrupt will clear upon reading this register.



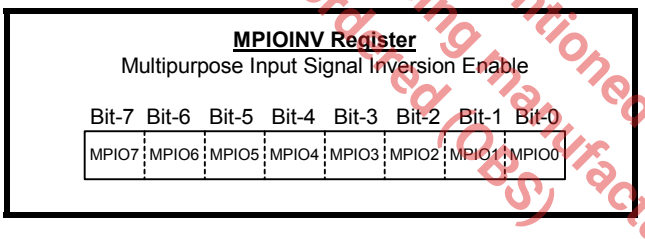

**MPIO3T [7:0] - (default 0x00)**

Output pin tri-state control. A logic 0 (default) sets the output to active level per register MPIOBIT settling, a logic 1 sets the output pin to tri-state.



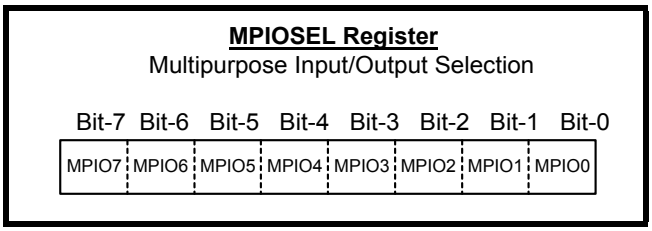

**MPIOINV [7:0] - (default 0x00)**

Input inversion control. A logic 0 (default) does not invert the input pin logic. A logic 1 inverts the input logic level.




**MPIOSEL [7:0] - (default 0xFF)**

Multipurpose input/output pin select. This register defines the functions of the pins. A logic 1 (default) defines the pin for input and a logic 0 for output.



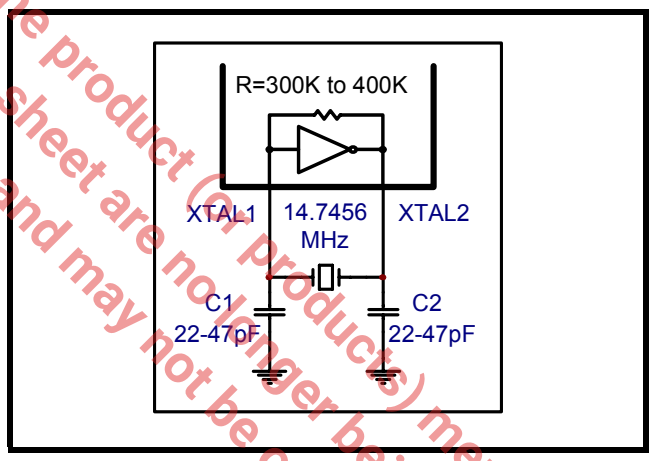

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## 3.0 CRYSTAL OSCILLATOR / BUFFER

The D154 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in each of the 4 UARTs, the 16-bit general purpose timer/counter and internal logics. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Caution: The XTAL1 input is not 5V tolerant. See Programmable Baud Rate Generator in the UART section for programming details.

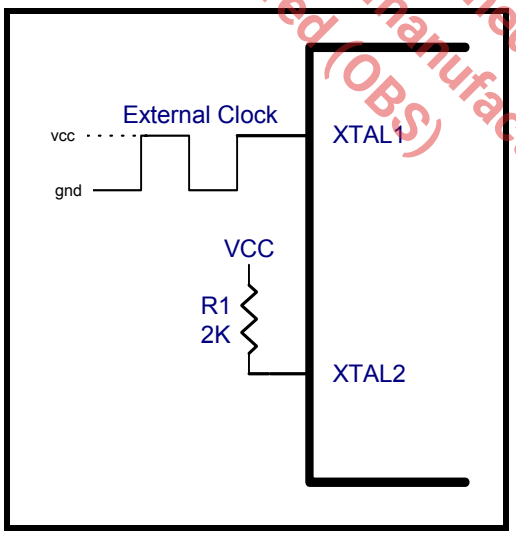
The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant with 10-22 pF capacitance load, 100ppm) connected externally between the XTAL1 and XTAL2 pins (see **Figure 9**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal 4 baud rate generators for standard or custom rates. However, for external clock frequencies greater than 24MHz, a 2K pull-up may be necessary on the XTAL2 output (see **Figure 10**). Typically, the oscillator connections are shown in **Figure 9**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

**FIGURE 9. TYPICAL OSCILLATOR CONNECTIONS**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**FIGURE 10. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE**



## 4.0 TRANSMIT AND RECEIVE DATA

There are two methods to load transmit data and unload receive data from each UART channel. First, there is a transmit data register and receive data register for each UART channel in the device configuration register set to ease programming. These registers support 8, 16, 24 and 32 bits wide format. In the 32-bit format, it increases the data transfer rate on the PCI bus. Additionally, a special register location provides receive data byte with its associated error flags. This is a 16-bit or 32-bit read operation where the Line Status Register (LSR) content in the UART channel register is paired along with the data byte. This operation further facilitates data unloading with the error flags without having to read the LSR register separately. Furthermore, the XR17D154 supports PCI burst mode for read/write operation of up to 64 bytes of data.

The second method is through each UART channel's transmit holding register (THR) and receive holding register (RHR). The THR and RHR registers are 16550 compatible so their access is limited to 8-bit format. The software driver must separately read the LSR content for the associated error flags before reading the data byte.

### *4.1 DATA LOADING AND UNLOADING VIA 32-BIT PCI BURST TRANSFERS*

The XR17D154 supports PCI Burst Read and PCI Burst Write transactions anywhere in the mapped memory region (except reserved areas). In addition, to utilize this feature fully, the device provides a separate memory location (apart from the 16550 register set) where the RX and the TX FIFO can be read from/written to, as shown in Table 3. The following is an extract from the table showing the burstable memory locations:

Channel 0:
- RX FIFO : 0x100 - 0x13F (64 bytes)
- TX FIFO : 0x100 - 0x13F (64 bytes)
- RX FIFO + status : 0x180 - 0x1FF (64 bytes data + 64 bytes status)

Channel 1:
- RX FIFO : 0x300 - 0x33F (64 bytes)
- TX FIFO : 0x300 - 0x33F (64 bytes)
- RX FIFO + status : 0x380 - 0x3FF (64 bytes data + 64 bytes status)

Channel 2:
- RX FIFO : 0x500 - 0x53F (64 bytes)
- TX FIFO : 0x500 - 0x53F (64 bytes)
- RX FIFO + status : 0x580 - 0x5FF (64 bytes data + 64 bytes status)

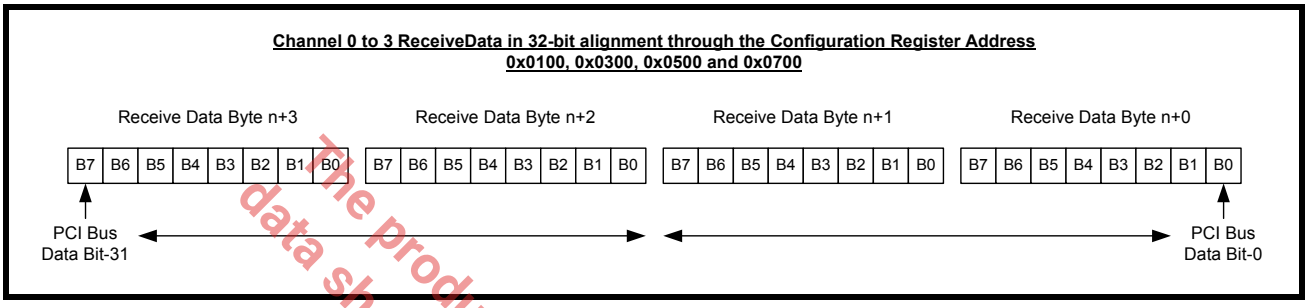
Channel 3:
- RX FIFO : 0x700 - 0x73F (64 bytes)
- TX FIFO : 0x700 - 0x73F (64 bytes)
- RX FIFO + status : 0x780 - 0x7FF (64 bytes data + 64 bytes status)

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

#### 4.1.1 Normal Rx FIFO Data Unloading at locations 0x100, 0x300, 0x500, 0x700

The RX FIFO data (up to the maximum 64 bytes) can be read out in a single burst 32-bit read operation (maximum 16 DWORD reads) at memory locations 0x100 (channel 0), 0x300 (channel 1), 0x500 (channel 2), and 0x700 (channel 3). This operation is at least 16 times faster than reading the data in 64 separate 8-bit memory reads of RHR register (0x000 for channel 0, 0x200 for channel 1, 0x400 for channel 2, and 0x600 for channel 3).

| READ RX FIFO, WITH NO ERRORS | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 |
|---|---|---|---|---|
| Read n+0 to n+3 | FIFO Data n+3 | FIFO Data n+2 | FIFO Data n+1 | FIFO Data n+0 |
| Read n+4 to n+7 | FIFO Data n+7 | FIFO Data n+6 | FIFO Data n+5 | FIFO Data n+4 |
| Etc. | | | | |

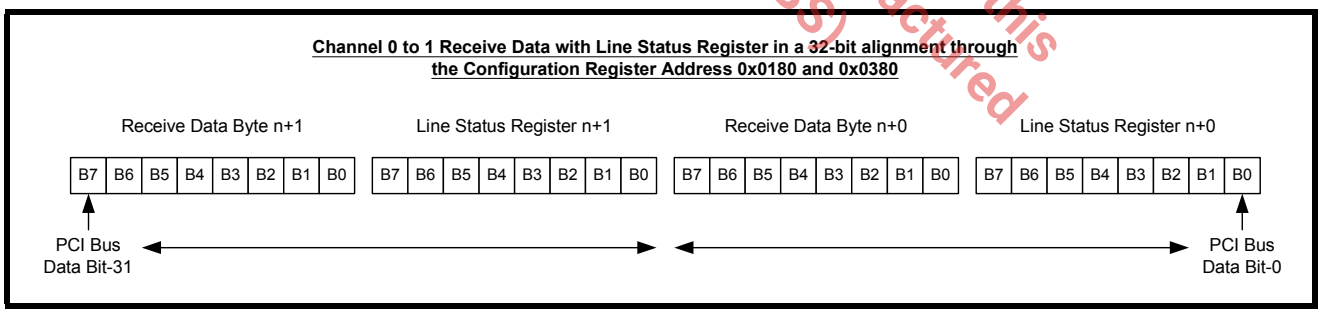



The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 4.1.2 Special Rx FIFO Data Unloading at locations 0x180, 0x380, 0x580, and 0x780

The XR17D154 also provides the same RX FIFO data along with the LSR status information of each byte side-by-side, at locations 0x180 (channel 0), 0x380 (channel 1), 0x580 (channel 2), and 0x780 (channel 3). The entire RX data along with the status can be downloaded in a single PCI Burst Read operation of 32 DWORD reads. The Status and Data bytes must be read in 16 or 32 bits format to maintain data integrity. The following tables show this clearly.

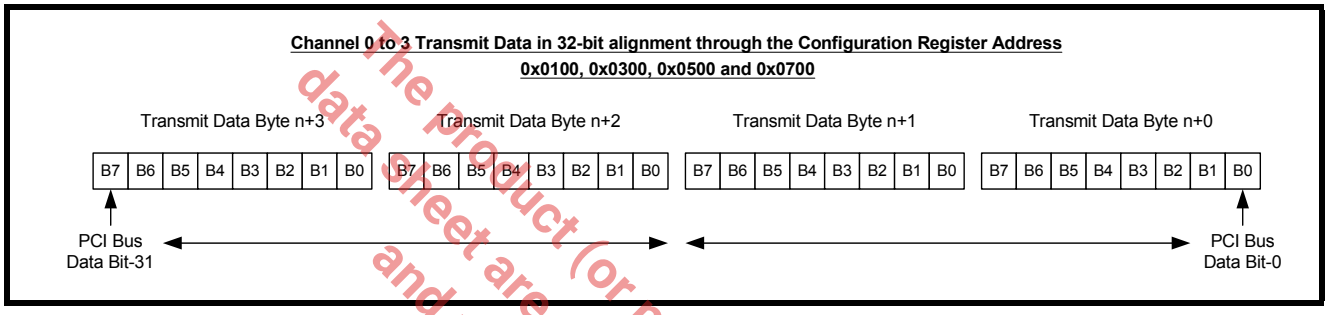
| READ RX FIFO, WITH LSR ERRORS | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 |
|---|---|---|---|---|
| Read n+0 to n+1 | FIFO Data n+1 | LSR n+1 | FIFO Data n+0 | LSR n+0 |
| Read n+2 to n+3 | FIFO Data n+3 | LSR n+3 | FIFO Data n+2 | LSR n+2 |
| Etc | | | | |



### 4.1.3 Tx FIFO Data Loading at locations 0x100, 0x300, 0x500, 0x700

The TX FIFO data (up to the maximum 64 bytes) can be loaded in a single burst 32-bit write operation (maximum 16 DWORD writes) at memory locations 0x100 (channel 0), 0x300 (channel 1), 0x500 (channel 2), and 0x700 (channel 3).

| WRITE TX FIFO | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 |
|---|---|---|---|---|
| Write n+0 to n+3 | FIFO Data n+3 | FIFO Data n+2 | FIFO Data n+1 | FIFO Data n+0 |
| Write n+4 to n+7 | FIFO Data n+7 | FIFO Data n+6 | FIFO Data n+5 | FIFO Data n+4 |
| Etc. | | | | |




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

## 4.2 FIFO DATA LOADING AND UNLOADING THROUGH THE UART CHANNEL REGISTERS, THR AND RHR IN 8-BIT FORMAT

The THR and RHR register address for channel 0 to channel 3 is shown in Table 9 below. The THR and RHR for each channel 0 to 3 are located sequentially at address 0x0000, 0x0200, 0x0400 and 0x0600. Transmit data byte is loaded to the THR when writing to that address and receive data is unloaded from the RHR register when reading that address. Both THR and RHR registers are 16C550 compatible in 8-bit format, so each bus operation can only write or read in bytes.

TABLE 9: TRANSMIT AND RECEIVE DATA REGISTER IN BYTE FORMAT, 16C550 COMPATIBLE

**THR and RHR Address Locations For CH0 to CH3 (16C550 Compatible)**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| CH0 | 0x000 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH0 | 0x000 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH1 | 0x200 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH1 | 0x200 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH2 | 0x400 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH2 | 0x400 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH3 | 0x600 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH3 | 0x600 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |

784THRRHR1

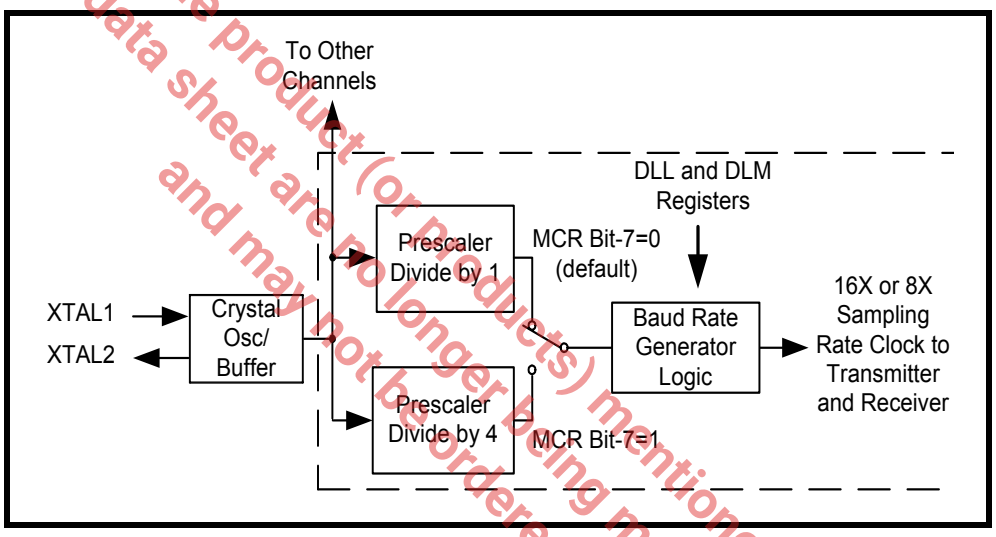
## 5.0 UART

There are 4 UARTs [channels 3:0] in the D154. Each has its own 64-byte of transmit and receive FIFO, a set of 16550 compatible control and status registers, and a baud rate generator for individual channel data rate setting. Eight additional registers per UART were added for the EXAR enhanced features.

### *5.1 Programmable Baud Rate Generator*

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and ($2^{16}$ -1) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up. Therefore, the BRG must be programmed during initialization to the operating data rate.

**FIGURE 11. BAUD RATE GENERATOR**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

Programming the Baud Rate Generator Registers DLM and DLL provides the capability for selecting the operating data rate. Table 10 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. At 8X sampling rate, these data rates would double. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s).

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), **WITH 8XMODE [3:0] IS 0**

divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 8), **WITH 8XMODE [3:0] IS 1**

TABLE 10: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

| OUTPUT Data Rate MCR Bit-7=1 | OUTPUT Data Rate MCR Bit-7=0 | DIVISOR FOR 16x Clock (Decimal) | DIVISOR FOR 16x Clock (HEX) | DLM PROGRAM VALUE (HEX) | DLL PROGRAM VALUE (HEX) | DATA RATE ERROR (%) |
|---|---|---|---|---|---|---|
| 100 | 400 | 2304 | 900 | 09 | 00 | 0 |
| 600 | 2400 | 384 | 180 | 01 | 80 | 0 |
| 1200 | 4800 | 192 | C0 | 00 | C0 | 0 |
| 2400 | 9600 | 96 | 60 | 00 | 60 | 0 |
| 4800 | 19.2k | 48 | 30 | 00 | 30 | 0 |
| 9600 | 38.4k | 24 | 18 | 00 | 18 | 0 |
| 19.2k | 76.8k | 12 | 0C | 00 | 0C | 0 |
| 38.4k | 153.6k | 6 | 06 | 00 | 06 | 0 |
| 57.6k | 230.4k | 4 | 04 | 00 | 04 | 0 |
| 115.2k | 460.8k | 2 | 02 | 00 | 02 | 0 |
| 230.4k | 921.6k | 1 | 01 | 00 | 01 | 0 |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

### *5.2 Transmitter*

The transmitter section comprises of a 64 bytes of FIFO, a byte-wide Transmit Holding Register (THR) and an 8-bit Transmit Shift Register (TSR). THR receives a data byte from the host (non-FIFO mode) or a data byte from the FIFO when the FIFO is enabled by FCR bit-0. TSR shifts out every data bit with the 16X or 8X internal clock. A bit time is 16 or 8 clock periods. The transmitter sends the start bit followed by the number of data bits, inserts the proper parity bit if enable, and adds the stop bit(s). The status of the THR and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

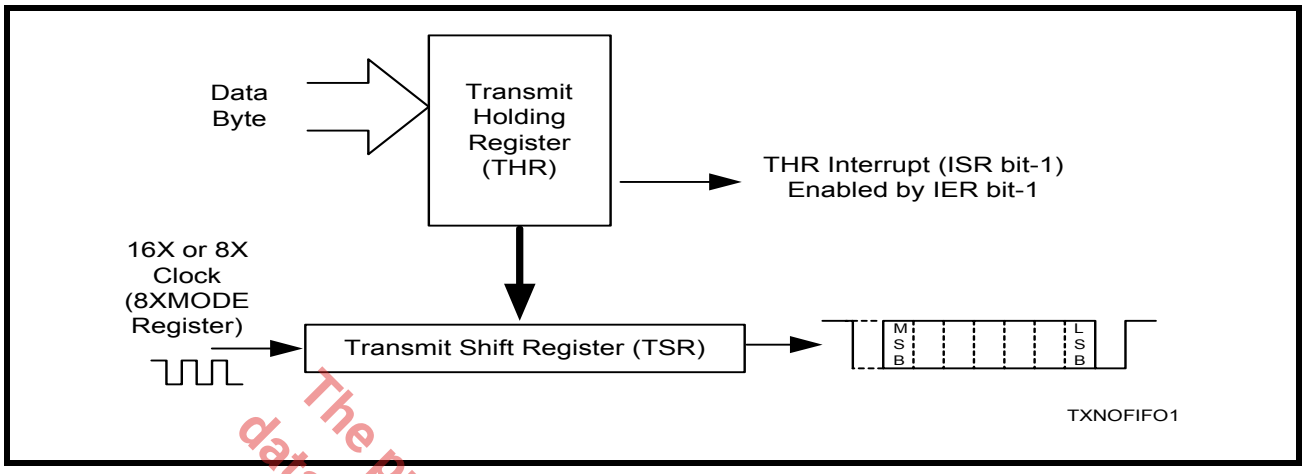
#### 5.2.1 Transmit Holding Register (THR) - Write-Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is also the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. A THR empty interrupt can be generated when it is enabled in IER bit-1.

#### 5.2.2 Transmitter Operation in non-FIFO mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 12. TRANSMITTER OPERATION IN NON-FIFO MODE




The product(s) mentioned in this data sheet are no longer in production and may not be manufactured or offered (OPS)

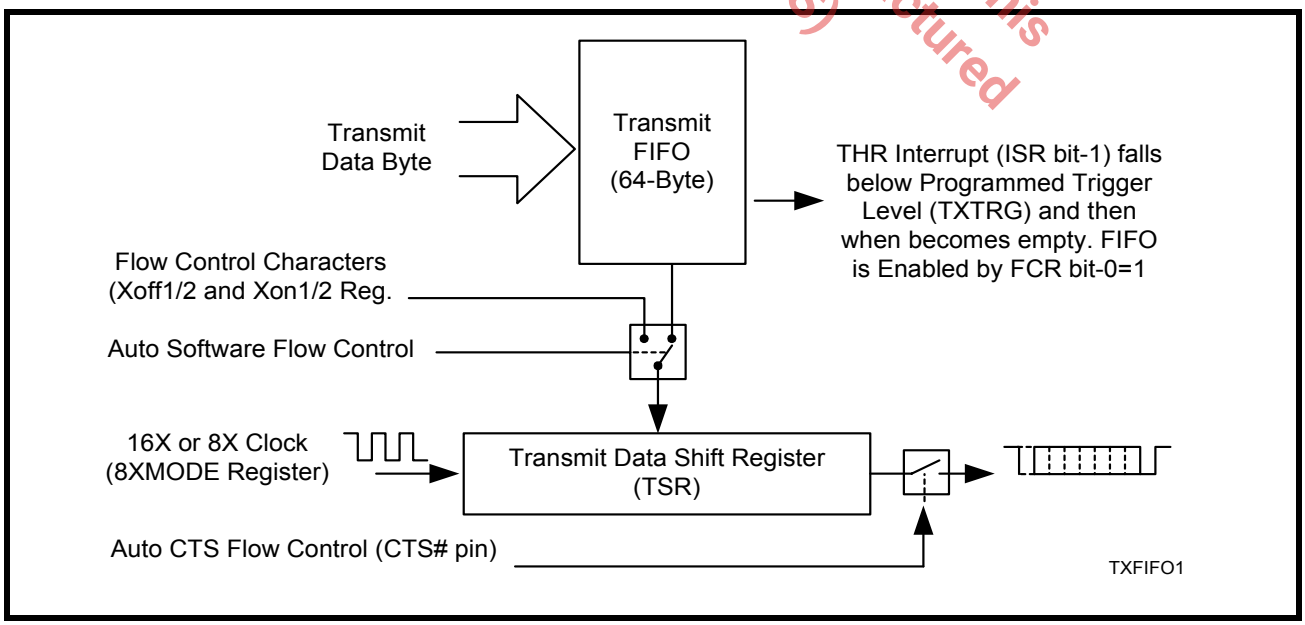
### 5.2.3 Transmitter Operation in FIFO mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level (see TXTRG register). The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty. Furthermore, with the RS485 half-duplex direction control enabled (FCTR bit-5=1) the source of the transmit empty interrupt changes to TSR empty instead of THR empty. This is to ensure the RTS# output is not changed until the last stop bit of the last character is shifted out.

### 5.2.4 Auto RS485 Operation

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-5. While transmitting, the RTS# or DTR# signal is HIGH. The RTS# or DTR# signal changes from HIGH to LOW after a specified delay indicated in MSR[7:4] following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver. This delay prevents undesirable line signal disturbance that causes signal degradation. It also changes the transmitter empty interrupt to TSR empty instead of THR empty.

FIGURE 13. TRANSMIITTER OPERATION IN FIFO AND FLOW CONTROL MODE



### 5.3 Receiver

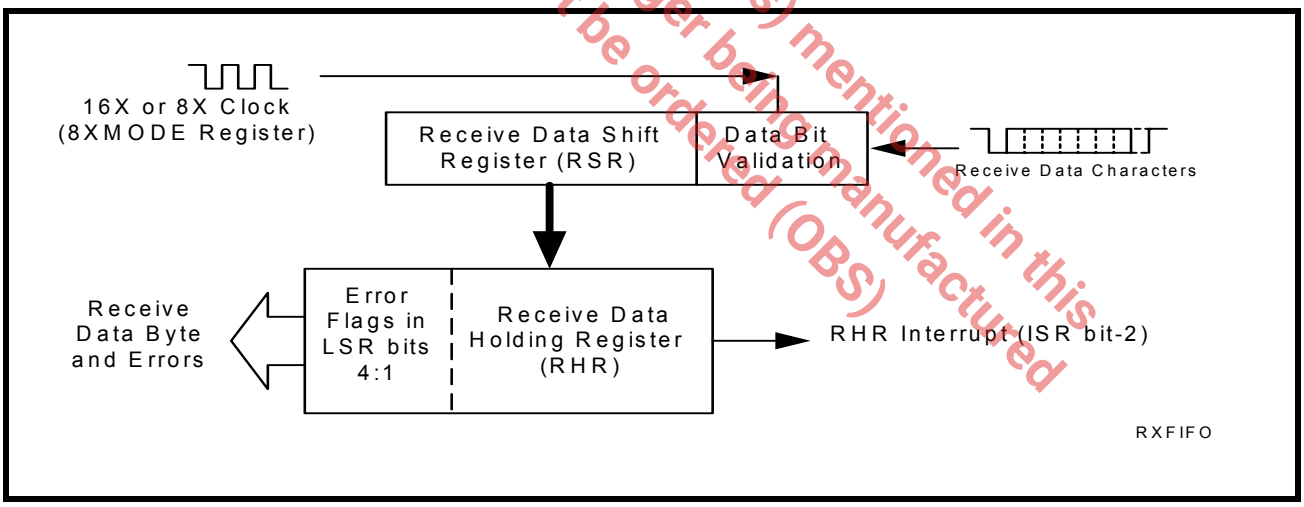
The receiver section contains an 8-bit Receive Shift Register (RSR) and Receive Holding Register (RHR). The RSR uses the 16X or 8X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X or 8X clock rate. After 8 or 4 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 1- 4 and an LSR interrupt is generated immediately if IER bit-2 is enabled. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out function when receive data does not reach the receive FIFO trigger level. This time-out delay is 4 word lengths as defined by LCR[1:0] plus 12 bits time. The RHR interrupt is enabled by IER bit-0.

#### 5.3.1 Receive Holding Register (RHR) - Read-Only

The receive holding register is an 8-bit register that holds a receive data byte from the receive shift register (RSR). It provides the receive data interface to the host processor. The host reads the receive data byte on this register whenever a data byte is transferred from the RSR. RHR also part of the receive FIFO of 64 bytes by 11-bit wide, 4 extra bits are for the error tags to be in LSR register. When the FIFO is enabled by FCR bit-0, it acts as the first-out register of the FIFO as new data are put over the first-in register. The receive FIFO pointer is bumped after the RHR register is read. Also, the error tags associated with the data byte are immediately updated onto the line status register (LSR) bits 1-4.

#### 5.3.2 Receiver Operation in non-FIFO Mode

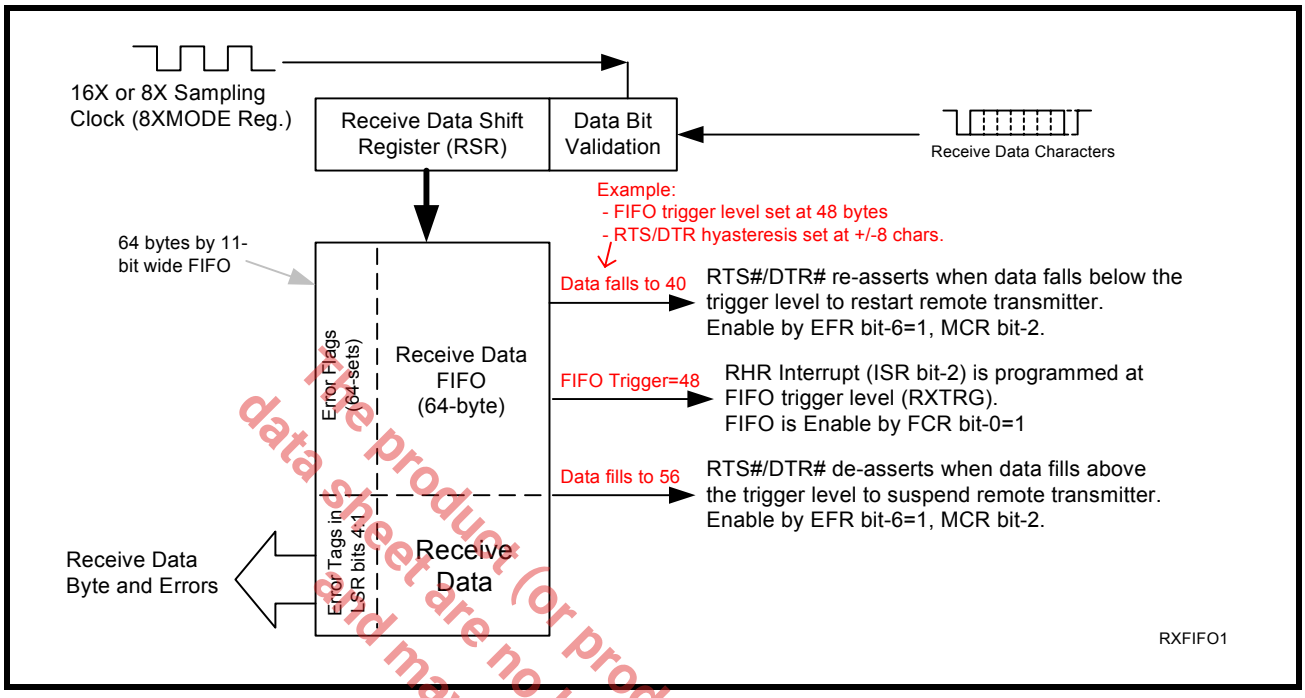
**FIGURE 14. RECEIVER OPERATION IN NON-FIFO MODE**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 5.3.3 Receiver Operation with FIFO

**FIGURE 15. RECEIVER OPERATION IN FIFO AND FLOW CONTROL MODE**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 5.4 *Automatic Hardware (RTS/CTS or DTR/DSR) Flow Control Operation*

Automatic hardware RTS/CTS or DTR/DSR flow control is used to prevent data overrun to the local receiver FIFO and remote receiver FIFO. The RTS#/DTR# output pin is used to request the remote unit to suspend/restart data transmission while the CTS#/DSR# input pin is monitored to suspend/restart the local transmitter. The auto RTS/CTS or DTR/DSR flow control features are individually selected to fit specific application requirement and enabled through EFR bit-6 and 7 and MCR bit-2 for either RTS/CTS or DTR/DSR control signals.

**TABLE 11: AUTO RTS/CTS OR DTR/DSR FLOW CONTROL SELECTION**

| MCR BIT-2 | EFR BIT-7 | EFR BIT-6 | HARDWARE FLOW CONTROL SELECTION |
|---|---|---|---|
| 0 | 1 | X | Auto CTS Flow Control Enabled |
| 0 | X | 1 | Auto RTS Flow Control Enabled |
| 1 | 1 | X | Auto DSR Flow Control Enabled |
| 1 | X | 1 | Auto DTR Flow Control Enabled |
| X | 0 | 0 | No Hardware Flow Control |

Auto RTS flow control must be started by asserting the RTS# output pin LOW (MCR bit-1 = 1). Similarly, Auto DTR flow control must be started by asserting the DTR# output pin LOW (MCR bit-0 = 1). **Figure 16** shows in detail how automatic hardware flow control works.

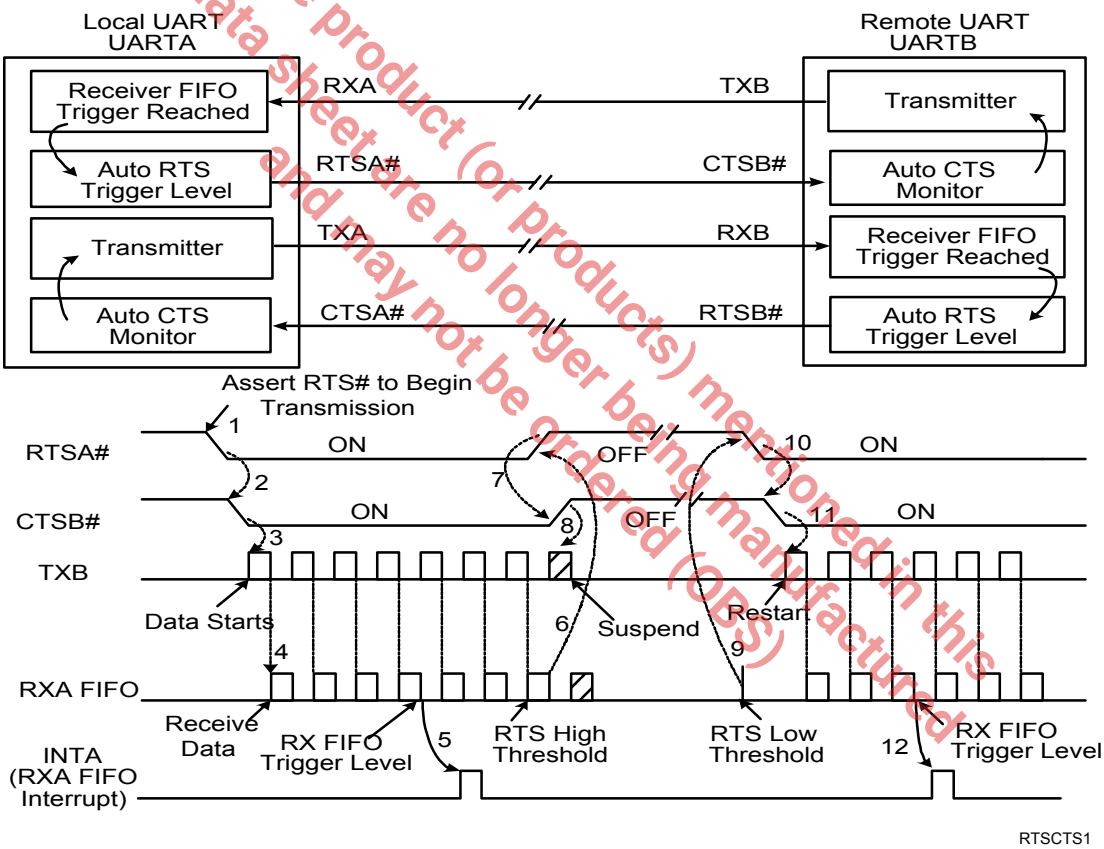
Two interrupts associated with auto RTS/CTS and DTR/DSR flow control have been added to give indication when RTS#/DTR# pin or CTS#/DSR# pin are de-asserted during operation. These interrupts are enabled by:

- Setting EFR bit-4 =1 to enable the shaded register bits
- Setting IER bit-7 will enable the CTS#/DSR# interrupt when these pins are de-asserted. The selection of CTS# or DSR# is selected via MCR bit-2. See **Table 11** above for complete details.
- Setting IER bit-6 will enable the RTS#/DTR# interrupt when these pins are de-asserted. The selection of RTS# or DTR# is selected via MCR bit-2. See **Table 11** above for complete details.

Automatic hardware flow control is selected by setting bits 6 (RTS) and 7 (CTS) of the EFR register to logic 1. If CTS# pin transitions from LOW to HIGH indicating a flow control request, ISR bit-5 will be set to logic 1, (if enabled via IER bit 6-7), and the UART will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input returns LOW, indicating more data may be sent.

**FIGURE 16. AUTO RTS/DTR AND CTS/DSR FLOW CONTROL OPERATION**

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)




*The local UART (UARTA) starts data transfer by asserting -RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.*

### 5.5 Infrared Mode

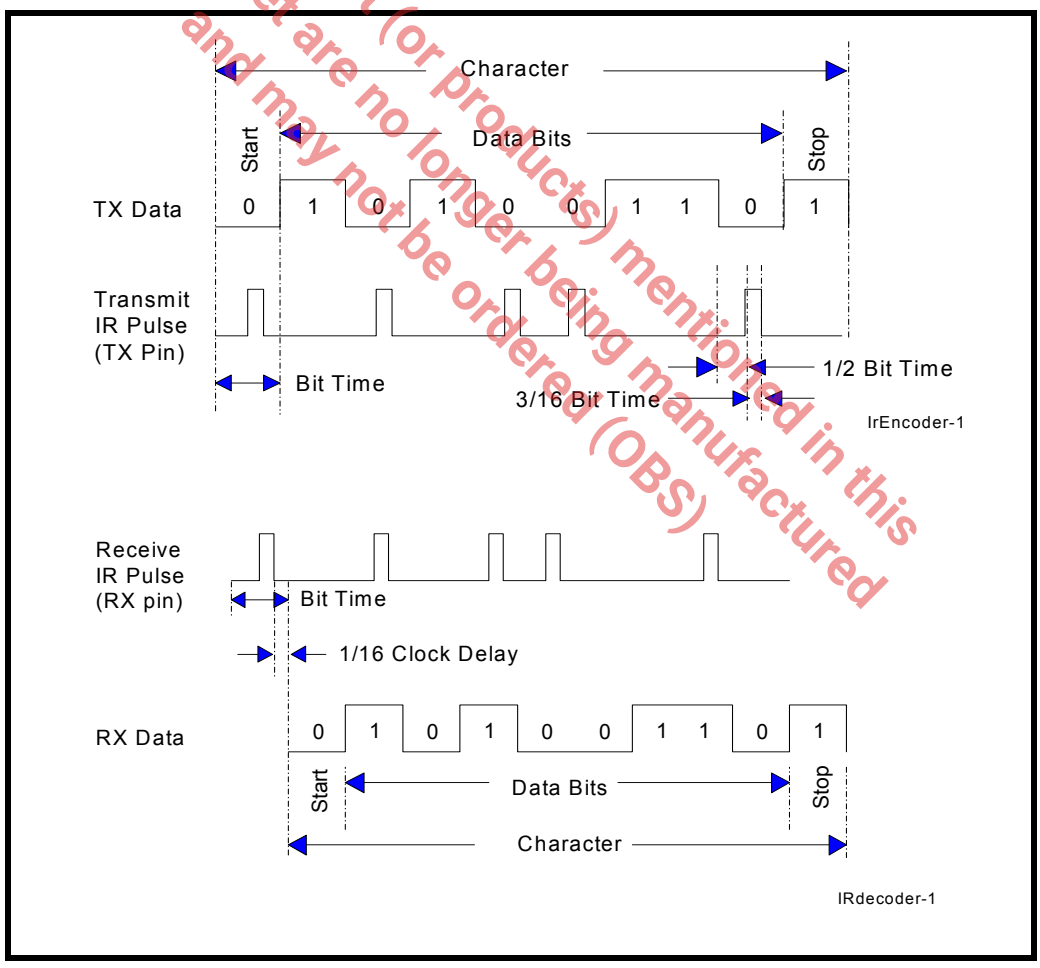
Each UART in the D154 includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The input pin ENIR conveniently activates all 4 UART channels to start up in the infrared mode. The ENIR pin is sampled when the RST# input is de-asserted. This global control pin enables the MCR bit-6 function in every UART channel register. After power up or a reset, the software can overwrite MCR bit-6 if so desired. ENIR and MCR bit-6 also disable its receiver while the transmitter is sending data. This prevents the echoed data from going to the receiver. The global activation ENIR pin prevents the infrared emitter from turning on and drawing large amount of current while the system is starting up. When the infrared feature is enabled, the transmit data outputs, TX[3:0], would idle at logic zero level. Likewise, the RX[3:0] inputs assume an idle level of logic zero.

The infrared encoder sends out a 3/16 of a bit wide pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 17 below.

The infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time it senses a light pulse, it returns a logic zero to the data bit stream. The RX input signal may be inverted prior delivered to the input of the decoder via internal register setting. This option supports active low instead of normal active high pulse from some infrared modules on the market.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

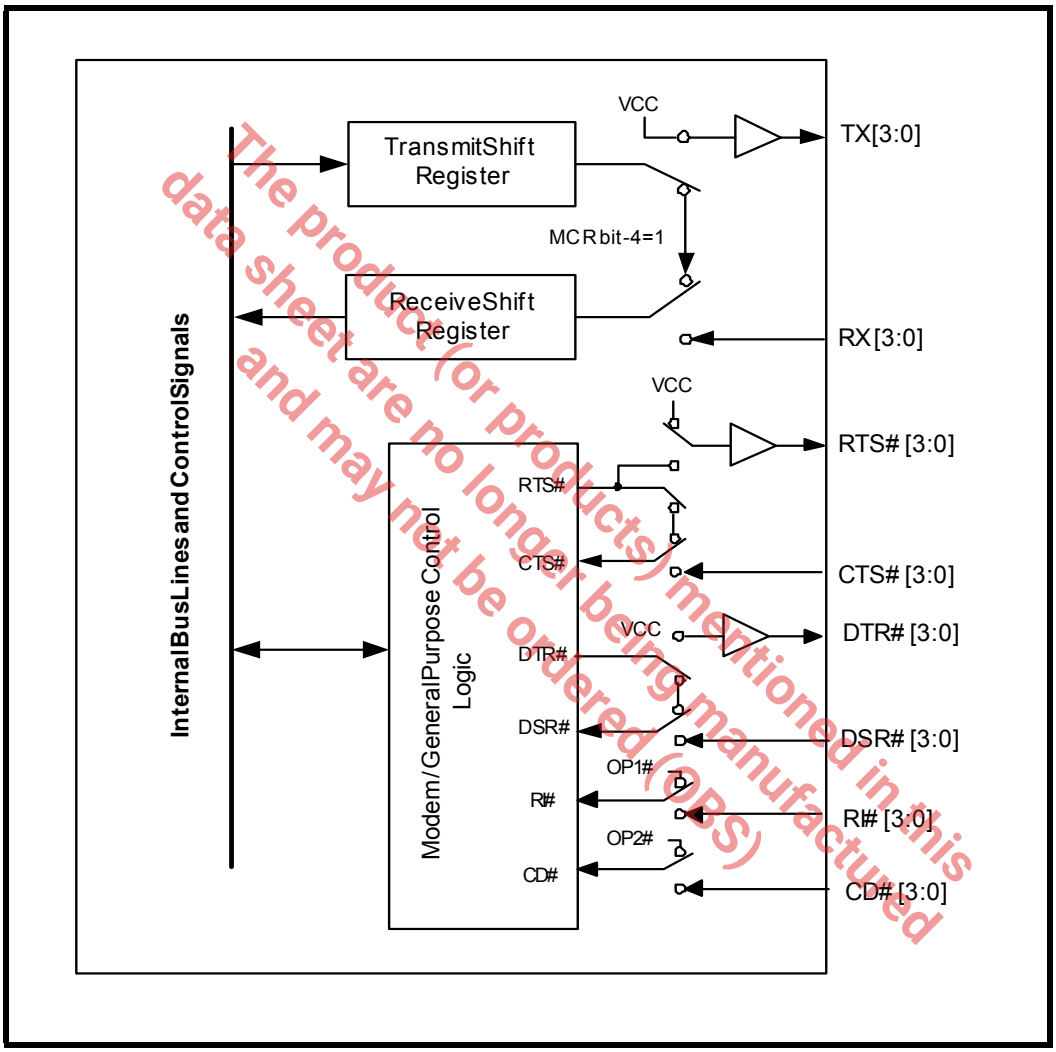
**FIGURE 17. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING**



### 5.6 Internal Loopback

Each UART channel provides an internal loopback capability for system diagnostic. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 18 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held HIGH (idle or de-asserted state), and the CTS#, DSR# CD# and RI# inputs are ignored.

**FIGURE 18. INTERNAL LOOP BACK**




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 5.7 UART CHANNEL CONFIGURATION REGISTERS AND ADDRESS DECODING

The 4 sets of UART configuration registers are decoded using address lines A9 to A11 as shown below:

| A11 | A10 | A9 | UART CHANNEL SELECTION |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |

Address lines A0 to A3 select the 16 registers in each channel. The first 8 registers are 16550 compatible with the EXAR enhanced feature registers located on next 8 addresses locations. Addresses 0x080 to 0x093 comprise the Device Configuration Registers and they reside in Channel 0's space.

**TABLE 12: UART CHANNEL CONFIGURATION REGISTERS**

| ADDRESS | | | | REGISTER | READ/WRITE | COMMENTS |
|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | | | |
| **16550 COMPATIBLE REGISTERS** | | | | | | |
| 0 | 0 | 0 | 0 | RHR - Receive Holding Register | Read-only | LCR[7] = 0 |
| 0 | 0 | 0 | 0 | THR - Transmit Holding Register | Write-only | LCR[7] = 0 |
| 0 | 0 | 0 | 0 | DLL - Div Latch Low | Read/Write | LCR[7] = 1 |
| 0 | 0 | 0 | 1 | DLM - Div Latch High | Read/Write | LCR[7] = 1 |
| 0 | 0 | 0 | 1 | IER - Interrupt Enable Register | Read/Write | LCR[7] = 0 |
| 0 | 0 | 1 | 0 | ISR - Interrupt Status Register | Read-only | |
| 0 | 0 | 1 | 0 | FCR - FIFO Control Register | Write-only | |
| 0 | 0 | 1 | 1 | LCR - Line Control Register | Read/Write | |
| 0 | 1 | 0 | 0 | MCR - Modem Control Register | Read/Write | |
| 0 | 1 | 0 | 1 | LSR - Line Status Register | Read-only | |
| 0 | 1 | 1 | 0 | MSR - Modem Status Register | Read-only | |
| 0 | 1 | 1 | 0 | RS485 Turn-Around Delay Register | Write-only | |
| 0 | 1 | 1 | 1 | SPR - Scratch Pad Register | Read/Write | |
| **ENHANCED REGISTERS** | | | | | | |
| 1 | 0 | 0 | 0 | FCTR - Feature Control Register | Read/Write | |
| 1 | 0 | 0 | 1 | EFR - Enhanced Function Register | Read/Write | |
| 1 | 0 | 1 | 0 | TXCNT - Transmit FIFO Level Counter | Read-only | |
| 1 | 0 | 1 | 0 | TXTRG - Transmit FIFO Trigger Level | Write-only | |
| 1 | 0 | 1 | 1 | RXCNT - Receive FIFO Level Counter | Read-only | |
| 1 | 0 | 1 | 1 | RXTRG - Receive FIFO Trigger Level | Write-only | |
| 1 | 1 | 0 | 0 | Xoff-1 - Xoff Character 1 | Write-only | |
| 1 | 1 | 0 | 0 | Xchar | Read-only | Xon,Xoff Rcvd. Flags |
| 1 | 1 | 0 | 1 | Xoff-2 - Xoff Character 2 | Write-only | |
| 1 | 1 | 1 | 0 | Xon-1 - Xon Character 1 | Write-only | |
| 1 | 1 | 1 | 1 | Xon-2 - Xon Character 2 | Write-only | |

The product(or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 13: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION.** SHADED BITS ARE ENABLED BY EFR BIT-4.

| ADDRESS A3-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 0 0 0 | RHR | R | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=0 |
| 0 0 0 0 | THR | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=0 |
| 0 0 0 0 | DLL | R/W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=1 |
| 0 0 0 1 | DLM | R/W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=1 |
| 0 0 0 1 | IER | R/W | 0/ CTS/ DSR# Int. Enable | 0/ RTS/ DTR# Int. Enable | 0/ Xon/Xoff/ Sp. Char. Int. Enable | 0 | Modem Status Int. Enable | RX Line Status Int. Enable | TX Empty Int. Enable | RX Data Int. Enable | |
| 0 0 1 0 | ISR | R | FIFOs Enable | FIFOs Enable | 0/ Delta-Flow Cntl | 0/ Xoff/special char | INT Source Bit-3 | INT Source Bit-2 | INT Source Bit-1 | INT Source Bit-0 | |
| 0 0 1 0 | FCR | W | RX FIFO Trigger | RX FIFO Trigger | 0/ TX FIFO Trigger | 0/ TX FIFO Trigger | DMA Mode | TX FIFO Reset | RX FIFO Reset | FIFOs Enable | |
| 0 0 1 1 | LCR | R/W | Divisor Enable | Set TX Break | Set Parity | Even Parity | Parity Enable | Stop Bits | Word Length Bit-1 | Word Length Bit-0 | |
| 0 1 0 0 | MCR | R/W | 0/ BRG Prescaler | 0/ IR Enable | 0/ XonAny | Internal Lopback Enable | (OP2)[1] | (OP1)[1] RTS/DTR Flow Sel | RTS# Pin Control | DTR# Pin Control | |
| 0 1 0 1 | LSR | R/W | RX FIFO ERROR | TSR Empty | THR Empty | RX Break | RX Framing Error | RX Parity Error | RX Over-run | RX Data Ready | |
| 0 1 1 0 | MSR | R | CD | RI | DSR | CTS | Delta CD# | Delta RI# | Delta DSR# | Delta CTS# | |
| | MSR | W | RS485 DLY-3 | RS485 DLY-2 | RS485 DLY-1 | RS485 DLY-0 | Reserved | Reserved | Reserved | Reserved | |
| 0 1 1 1 | SPR | R/W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | User Data |
| 1 0 0 0 | FCTR | R/W | TRG Table Bit-1 | TRG Table Bit-0 | Auto RS485 Enable | Invert IR RX Input | RTS/DTR Hyst Bit-3 | RTS/DTR Hyst Bit-2 | RTS/DTR Hyst Bit-1 | RTS/DTR Hyst Bit-0 | |
| 1 0 0 1 | EFR | R/W | Auto CTS/DSR Enable | Auto RTS/DTR Enable | Special Char Select | Enable IER [7:5], ISR [5:4], FCR[5:4], MCR[7:5,2] MSR[7:4] | Software Flow Cntl Bit-3 | Software Flow Cntl Bit-2 | Software Flow Cntl Bit-1 | Software Flow Cntl Bit-0 | |
| 1 0 1 0 | TXCNT | R | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 0 | TXTRG | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 1 | RXCNT | R | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 1 | RXTRG | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

The Product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 13: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION.** SHADED BITS ARE ENABLED BY EFR BIT-4.

| ADDRESS A3-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 1 0 0 | XCHAR | R | 0 | 0 | 0 | 0 | 0 | 0 | Xon Det. Indicator | Xoff Det. Indicator | Self-clear after read |
| 1 1 0 0 | XOFF1 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 0 1 | XOFF2 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 1 0 | XON1 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 1 1 | XON2 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

*NOTE: MCR bits 2 and 3 (OP1 and OP2 outputs) are not available in the XR17D154. They are present for 16C550 compatibility during Internal loopback, see* Figure 18.

The Product(or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## 5.8 Registers

### 5.8.1 Receive Holding Register (RHR) - Read-Only

See "Section 5.3, Receiver" on page 30 for complete details.

### 5.8.2 Transmit Holding Register (THR) - Write-Only

See "Section 5.2, Transmitter" on page 28 for complete details.

### 5.8.3 Baud Rate Generator Divisors (DLL and DLM) - Read/Write

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter and receiver. The baud rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to logic 1. See "Section 5.1, Programmable Baud Rate Generator" on page 27 for more detail.

### 5.8.4 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) register and also encoded in INT (INT0-INT3) register in the Device Configuration Registers.

#### IER VERSUS RECEIVE FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR bit-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 3 and 4) status will reflect the following:

**A.** The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

**B.** FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

**C.** The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

#### IER VERSUS RECEIVE/TRANSMIT FIFO POLLED MODE OPERATION

When FCR BIT-0 equals a logic 1 for FIFO enable, resetting IER bits 0-3 enables the 158 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

**A.** LSR BIT-0 indicates there is data in RHR or RX FIFO.

**B.** LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

**C.** LSR BITS 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

**D.** LSR BIT-5 indicates THR is empty.

**E.** LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

**F.** LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

**IER[0]: RHR Interrupt Enable**

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode. A receive data timeout interrupt will be issued in the FIFO mode when the receive FIFO has not reached the programmed trigger level and the RX input has been idle for 4 character + 12 bit times.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

**IER[1]: THR Interrupt Enable**

When Auto RS485 mode operation is disabled (FCTR bit-5 = 0), this interrupt is associated with bit-5 in the LSR register. An interrupt is issued whenever the THR becomes empty or when data in the FIFO falls below the programmed trigger level. When Auto RS485 mode operation is enabled (FCTR bit-5 = 1), this interrupt is associated with bit-6 in the LSR register. An interrupt is issued whenever the TX FIFO and the TSR becomes empty.

- Logic 0 = Disable Transmit Holding Register empty interrupt (default).
- Logic 1 = Enable Transmit Holding Register empty interrupt.

**IER[2]: Receive Line Status Interrupt Enable**

Any of LSR register bits 1, 2, 3 or 4 will generate an LSR interrupt immediately when a character received by the RX FIFO has an error.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

**IER[3]: Modem Status Interrupt Enable**

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

**IER[4]: Reserved**

**IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)**

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

**IER[6]: RTS#/DTR# Output Interrupt Enable (requires EFR bit-4=1)**

The RTS# or DTR# output is selected via MCR bit-2. See Table 11 or MCR[2] for complete details.

- Logic 0 = Disable the RTS#/DTR# interrupt (default).
- Logic 1 = Enable the RTS#/DTR# interrupt. The UART issues an interrupt when the RTS#/DTR# pin makes a transition.

**IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)**

The CTS# or DSR# input is selected via MCR bit-2. See Table 11 or MCR[2] for complete details.

- Logic 0 = Disable the CTS#/DSR# interrupt (default).
- Logic 1 = Enable the CTS#/DSR# interrupt. The UART issues an interrupt when CTS# pin makes a transition.

### 5.8.5 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced with others queued up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 14, shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**Interrupt Generation:**

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by the a 4-char plus 12 bits delay timer if the RX FIFO level is less than the RX trigger level.
- TXRDY is by LSR bit-5 (or bit-6 in auto RS485 control).
- MSR is by any of the MSR bits, 0, 1, 2 and 3.
- Receive Xon/Xoff/Special character is by detection of a Xon, Xoff or Special character.
- CTS#/DSR# is by a change of state on the input pin (from LOW to HIGH) with auto flow control enabled, EFR bit-7, and depending on selection of MCR bit-2.
- RTS#/DTR# is when its receiver changes the state of the output pin (from LOW to HIGH) during auto RTS/DTR flow control enabled by EFR bit-6 and selection of MCR bit-2.
- Wake-up Indicator: when the UART comes out of sleep mode.

**Interrupt Clearing:**

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out is cleared by reading data until the RX FIFO is empty.
- TXRDY interrupt is cleared by a read to the ISR register.
- MSR interrupt is cleared by a read to the MSR register.
- Xon or Xoff character interrupt is cleared by a read to ISR register.
- Special character interrupt is cleared by a read to ISR register or after the next character is received.
- RTS#/DTR# and CTS#/DSR# status change interrupts are cleared by a read to the MSR register.
- Wake-up Indicator is cleared by a read to the INT0 register.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 14: INTERRUPT SOURCE AND PRIORITY LEVEL**

| PRIORITY LEVEL | ISR REGISTER STATUS BITS | | | | | | SOURCE OF THE INTERRUPT |
|---|---|---|---|---|---|---|---|
| | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | LSR (Receiver Line Status Register) |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | RXRDY (Received Data Ready) |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | RXRDY (Receive Data Time-out) |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 | TXRDY (Transmitter Holding Register Empty) |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | MSR (Modem Status Register) |
| 6 | 0 | 1 | 0 | 0 | 0 | 0 | RXRDY (Received Xon/Xoff or Special character) |
| 7 | 1 | 0 | 0 | 0 | 0 | 0 | CTS#/DSR#, RTS#/DTR# change of state |
| X | 0 | 0 | 0 | 0 | 0 | 1 | None (default) |

**ISR[0]: Interrupt Status**

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

**ISR[3:1]: Interrupt Status**

These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, 3 and 4 (See Interrupt Source Table 14).

**ISR[4]: Xoff/Xon or Special Character Interrupt Status**

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). If this is an Xoff/Xon interrupt, it can be cleared by a read to the ISR. Reading the XCHAR register will indicate which character (Xoff or Xon) was received last. If it is a special character interrupt, it can be cleared by reading ISR or it will automatically clear after the next character is received.

**ISR[5]: RTS#/CTS# Interrupt Status**

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-5 indicates that the CTS# or RTS# has changed state from LOW to HIGH.

**ISR[7:6]: FIFO Enable Status**

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

### 5.8.6 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode (legacy term that refers to "block transfer mode"). The DMA and FIFO modes are defined as follows:

**FCR[0]: TX and RX FIFO Enable**

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

**FCR[1]: RX FIFO Reset**

This bit is only active when FCR bit-0 is active.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

**FCR[2]: TX FIFO Reset**

This bit is only active when FCR bit-0 is active.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

**FCR[3]: DMA Mode Select**

This bit has no effect since TXRDY and RXRDY pins are not available in this device. It is provided for legacy software. DMA is a legacy term used for block transfer mode. DMA does not stand for "Direct Memory Access."

- Logic 0 = Set DMA to mode 0 (default).
- Logic 1 = Set DMA to mode 1.

**FCR[5:4]: Transmit FIFO Trigger Select**

(logic 0 = default, TX trigger level = 1)

The FCTR bits 6-7 are associated with these 2 bits by selecting one of the four tables. The 4 user selectable trigger levels in 4 tables are supported for compatibility reasons. These 2 bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 15 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

The product (or product) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**FCR[7:6]: Receive FIFO Trigger Select**

(logic 0 = default, RX trigger level =1)

The FCTR Bits 6-7 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receiver FIFO interrupt. Table 15 shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

**TABLE 15: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION**

| TRIGGER TABLE | FCTR BIT-7 | FCTR BIT-6 | FCR BIT-7 | FCR BIT-6 | FCR BIT-5 | FCR BIT-4 | RECEIVE TRIGGER LEVEL | TRANSMIT TRIGGER LEVEL | COMPATIBILITY |
|---|---|---|---|---|---|---|---|---|---|
| **Table A** | 0 | 0 | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | 0 | 0 | 1 (default)<br>4<br>8<br>14 | 1 (default) | 16C550, 16C2550, 16C2552, 16C554, 16C580 compatible. |
| **Table B** | 0 | 1 | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | 8<br>16<br>24<br>28 | 16<br>8<br>24<br>30 | 16C650A compatible. |
| **Table C** | 1 | 0 | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | 8<br>16<br>56<br>60 | 8<br>16<br>32<br>56 | 16C654 compatible. |
| **Table D** | 1 | 1 | X | X | X | X | Programmable | Programmable | 16C850, 16C2850, 16C2852, 16C854, 16C864, 16L2750, 16L2751, 16L2752 compatible. |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

### 5.8.7 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

**LCR[1:0]: TX and RX Word Length Select**

These two bits specify the word length to be transmitted or received.

| BIT-1 | BIT-0 | WORD LENGTH |
|---|---|---|
| 0 | 0 | 5 (default) |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

**LCR[2]: TX and RX Stop-bit Length Select**

The length of stop bit is specified by this bit in conjunction with the programmed word length.

| BIT-2 | WORD LENGTH | STOP BIT LENGTH (BIT TIME(S)) |
|---|---|---|
| 0 | 5,6,7,8 | 1 (default) |
| 1 | 5 | 1-1/2 |
| 1 | 6,7,8 | 2 |

**LCR[3]: TX and RX Parity Select**

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 16 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

**LCR[4]: TX and RX Parity Select**

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

**LCR[5]: TX and RX Parity Select**

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 16: PARITY SELECTION

| LCR BIT-5 | LCR BIT-4 | LCR BIT-3 | PARITY SELECTION |
|---|---|---|---|
| X | X | 0 | No parity |
| 0 | 0 | 1 | Odd parity |
| 0 | 1 | 1 | Even parity |
| 1 | 0 | 1 | Force parity to mark, “1” |
| 1 | 1 | 1 | Forced parity to space, “0” |

**LCR[6]: Transmit Break Enable**

When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a “space", LOW state). This condition remains until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a “space”, LOW, for alerting the remote receiver of a line break condition.

**LCR[7]: Baud Rate Divisors Enable**

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

### 5.8.8 Modem Control Register (MCR) - Read/Write

The MCR register is used for controlling the modem interface signals or general purpose inputs/outputs.

**MCR[0]: DTR# Pins**

The DTR# pin may be used for automatic hardware flow control enabled by EFR bit-6 and MCR bit-2=1. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

**MCR[1]: RTS# Pins**

The RTS# pin may be used for automatic hardware flow control by enabled by EFR bit-6 and MCR bit-2=0. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force RTS# output HIGH (default).
- Logic 1 = Force RTS# output LOW.

**MCR[2]: DTR# or RTS# for Auto Flow Control**

DTR# or RTS# auto hardware flow control select. This bit is in effect only when auto RTS/DTR is enabled by EFR bit-6. DTR# selection is associated with DSR# and RTS# is with CTS#.

- Logic 0 = Uses RTS# and CTS# pins for auto hardware flow control.
- Logic 1 = Uses DTR# and DSR# pins for auto hardware flow control.

**MCR[3]: (OP2)**

The OP2 output is not available in the XR17D154. It is present for 16C550 compatibility during internal loopback. See Figure 18. Logic 0 is default.

**MCR[4]: Internal Loopback Enable**

- Logic 0 = Disable internal loopback mode (default).
- Logic 1 = Enable internal loopback mode, see loopback section and Figure 18.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**MCR[5]: Xon-Any Enable**

- Logic 0 = Disable Xon-Any function (for 16C550 compatibility) (default).
- Logic 1 = Enable Xon-Any function. In this mode any RX character received will enable Xon, resume data transmission.

**MCR[6]: Infrared Encoder/Decoder Enable**

The state of this bit depends on the sampled logic level of pin ENIR during power up, following a hardware reset or a soft-reset. Afterward user can override this bit for desired operation.

- Logic 0 = Disable the infrared mode, operates in the normal serial character mode.
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions. FCTR bit-4 may be selected to invert the RX input signal level going to the decoder for infrared modules that provide rather an inverted output.

**MCR[7]: Clock Prescaler Select**

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one-fourth.

### 5.8.9 Line Status Register (LSR) - Read/Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is set to a logic 1, an LSR interrupt will be generated immediately when any character in the RX FIFO has an error (parity, framing, overrun, break). Reading LSR will clear LSR bits 4-1.

**LSR[0]: Receive Data Ready Indicator**

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

**LSR[1]: Receiver Overrun Flag**

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error. This bit is cleared after LSR is read.

**LSR[2]: Receive Data Parity Error Tag**

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR. This bit is cleared after LSR is read.

**LSR[3]: Receive Data Framing Error Tag**

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR. This bit is cleared after LSR is read.

**LSR[4]: Receive Break Tag**

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. This bit is cleared after LSR is read.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**LSR[5]: Transmit Holding Register Empty Flag**

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the host when the THR interrupt enable is set. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

**LSR[6]: Transmit Shift Register Empty Flag**

This bit is the Transmit Shift Register Empty indicator. This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

**LSR[7]: Receive FIFO Data Error Flag**

- Logic 0 = No FIFO error (default).
- Logic 1 = An indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in the FIFO.

### 5.8.10 Modem Status Register (MSR) - Read-Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

**MSR[0]: Delta CTS# Input Flag**

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

**MSR[1]: Delta DSR# Input Flag**

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

**MSR[2]: Delta RI# Input Flag**

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

**MSR[3]: Delta CD# Input Flag**

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

**MSR[4]: CTS Input Status**

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7) and RTS/CTS flow control select (MCR bit-2). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A logic 1 on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a logic 0 will resume data transmission. If automatic hardware flow control is not used, MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

**MSR[5]: DSR Input Status**

This input may be used for auto DTR/DSR flow control function, see **"Section 5.4, Automatic Hardware (RTS/CTS or DTR/DSR) Flow Control Operation" on page 31** for complete details. If automatic hardware flow control is not used, this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

**MSR[6]: RI Input Status**

This bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

**MSR[7]: CD Input Status**

This bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input

### 5.8.11 Modem Status Register (MSR) - Write-Only

The upper four bits 4-7 of this register sets the delay in number of bits time for the auto RS485 turn around from transmit to receive.

**MSR [7:4]**

When Auto RS485 feature is enabled (FCTR bit-5=1) and RTS# output is connected to the enable input of a RS-485 transceiver. These 4 bits select from 0 to 15 bit-time delay after the end of the last stop-bit of the last transmitted character. This delay controls when to change the state of RTS# output. This delay is very useful in long-cable networks. Table 17 shows the selection. The bits are enabled by EFR bit-4.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**TABLE 17: AUTO RS485 HALF-DUPLEX DIRECTION CONTROL DELAY FROM TRANSMIT-TO-RECEIVE**

| MSR[7] | MSR[6] | MSR[5] | MSR[4] | DELAY IN DATA BIT(S) TIME |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 9 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |

### 5.8.12 SCRATCH PAD REGISTER (SPR) - Read/Write

This is an 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

### 5.8.13 FEATURE CONTROL REGISTER (FCTR) - Read/Write

**FCTR [3:0] - Auto RTS/DTR Flow Control Hysteresis Select**

These bits select the auto RTS/DTR flow control hysteresis and only valid when TX and RX Trigger Table-D is selected (FCTR bit-6 and 7 are set to logic 1). The RTS/DTR hysteresis is referenced to the RX FIFO trigger level. After reset, these bits are set to logic 0 selecting the next FIFO trigger level for hardware flow control. Table 18 shows the 16 selectable hysteresis levels.

**FCTR[4]: Infrared RX Input Logic Select**

- Logic 0 = Select RX input as active high encoded IrDA data, normal, (default).
- Logic 1 = Select RX input as active low encoded IrDA data, inverted.

**FCTR[5]: Auto RS485 Enable**

Auto RS485 half duplex control enable/disable.

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register (THR) becomes empty. Transmit Shift Register (TSR) may still be shifting data bit out.
- Logic 1 = Enable Auto RS485 half duplex direction control. RTS# output changes its logic level from HIGH to LOW when finished sending the last stop bit of the last character out of the TSR register. It changes back to HIGH from LOW when a data byte is loaded into the THR or transmit FIFO. The change to HIGH occurs prior sending the start-bit. It also changes the transmitter interrupt from transmit holding to transmit shift register (TSR) empty.

**FCTR[7:6]: TX and RX FIFO Trigger Table Select**

These 2 bits select the transmit and receive FIFO trigger level table A, B, C or D. When table A, B, or C is selected the auto RTS flow control trigger level is set to "next FIFO trigger level" for compatibility to ST16C550 and ST16C650 series. RTS#/DTR# triggers on the next level of the RX FIFO trigger level, in another word, one FIFO level above and one FIFO level below. See Table 15 for complete selection with FCR bit 4-5 and FCTR bit 6-7, i.e. if Table C is used on the receiver with RX FIFO trigger level set to 56 bytes, RTS/DTR# output will de-assert at 60 and re-assert at 16.

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be offered (OBS)

TABLE 18: 16 SELECTABLE HYSTERESIS LEVELS WHEN TRIGGER TABLE-D IS SELECTED

| FCTR BIT-3 | FCTR BIT-2 | FCTR BIT-1 | FCTR BIT-0 | RTS/DTR HYSTERESIS (CHARACTERS) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | ± 4 |
| 0 | 0 | 1 | 0 | ± 6 |
| 0 | 0 | 1 | 1 | ± 8 |
| 0 | 1 | 0 | 0 | ± 8 |
| 0 | 1 | 0 | 1 | ± 16 |
| 0 | 1 | 1 | 0 | ± 24 |
| 0 | 1 | 1 | 1 | ± 32 |
| 1 | 0 | 0 | 0 | ± 12 |
| 1 | 0 | 0 | 1 | ± 20 |
| 1 | 0 | 1 | 0 | ± 28 |
| 1 | 0 | 1 | 1 | ± 36 |
| 1 | 1 | 0 | 0 | ± 40 |
| 1 | 1 | 0 | 1 | ± 44 |
| 1 | 1 | 1 | 0 | ± 48 |
| 1 | 1 | 1 | 1 | ± 52 |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 5.8.14 Enhanced Feature Register (EFR) - Read/Write

Enhanced features are enabled or disabled using this register. Bits 0-3 provide single or dual consecutive character software flow control selection (see Table 19). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

**EFR[3:0]: Software Flow Control Select**

Combinations of software flow control can be selected by programming these bits. See Table 19 for complete selections. The XOFF1/XOFF2 characters are transmitted approximately 2 character times after the RX FIFO level has reached the RX trigger level, irrespective of which trigger table is used (Trigger Tables A-D). The XON1/XON2 characters are transmitted when the RX FIFO level falls below the next lower trigger level for Trigger Tables A-C and they are transmitted when the RX FIFO level falls below the (RX trigger level - hysteresis level) for Trigger Table D. For example, if Trigger Table D is used with an RX trigger level of 56 and a hysteresis level of 16, the XON1/XON2 characters are sent when the RX FIFO level count falls below 40.

**EFR[4]: Enhanced Function Bits Enable**

Enhanced function control bit. This bit enables the functions in IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with the industry standard 16550 (default).
- Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1 all enhanced features are enabled.

**EFR[5]: Special Character Detect Enable**

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit for the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]='10') then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]='01') then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OPS).

**TABLE 19: SOFTWARE FLOW CONTROL FUNCTIONS**

| TX S/W FLOW CONTROL | | RX S/W FLOW CONTROL | | |
|---|---|---|---|---|
| EFR BIT-3 CONT-3 | EFR BIT-2 CONT-2 | EFR BIT-1 CONT-1 | EFR BIT-0 CONT-0 | SOFTWARE FLOW CONTROL FUNCTIONS |
| 0 | 0 | X | X | No transmit flow control |
| 0 | 1 | X | X | Transmit Xon2, Xoff2 |
| 1 | 0 | X | X | Transmit Xon1, Xoff1 |
| 1 | 1 | X | X | Transmit Xon1 and Xon2, Xoff1 and Xoff2 |
| X | X | 0 | 0 | No receive flow control |
| X | X | 0 | 1 | Receiver compares Xon2, Xoff2 |
| X | X | 1 | 0 | Receiver compares Xon1, Xoff1 |
| 0 | 1 | 1 | 1 | Transmit Xon2, Xoff2<br>Receiver compares Xon1 or Xon2, Xoff1 or Xoff2 |
| 1 | 0 | 1 | 1 | Transmit Xon1, Xoff1<br>Receiver compares Xon1 or Xon2, Xoff1 or Xoff2 |
| 0 | 0 | 1 | 1 | No transmit flow control<br>Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 |
| 1 | 1 | 1 | 1 | Transmit Xon1 and Xon2, Xoff1 and Xoff2<br>Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 |

**EFR[6]: Auto RTS or DTR Flow Control Enable**

RTS#/DTR# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS/DTR is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS#/DTR# will de-assert HIGH at the next upper trigger or selected hysteresis level. RTS#/DTR# will return LOW when FIFO data falls below the next lower trigger or selected hysteresis level (see FCTR bits 4-7). The RTS# or DTR# output must be asserted (LOW) before the auto RTS/DTR can take effect. The selection for RTS# or DTR# is through MCR bit-2. RTS/DTR# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS/DTR flow control is disabled (default).
- Logic 1 = Enable Automatic RTS/DTR flow control.

**EFR[7]: Auto CTS Flow Control Enable**

Automatic CTS or DSR Flow Control.

- Logic 0 = Automatic CTS/DSR flow control is disabled (default).
- Logic 1 = Enable Automatic CTS/DSR flow control. Transmission stops when CTS#/DSR# pin de-asserts HIGH. Transmission resumes when CTS/DSR# pin returns LOW. The selection for CTS# or DSR# is through MCR bit-2.

### 5.8.15 TXCNT[7:0]: Transmit FIFO Level Counter - Read-Only

Transmit FIFO level byte count from 0x00 (zero) to 0x40 (64). This 8-bit register gives an indication of the number of characters in the transmit FIFO. The FIFO level Byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data loading to the transmit FIFO, which reduces CPU bandwidth requirements. Please see the Application Note DAN119 on Exar's website for a detailed discussion of FIFO level counters. Due to the dynamic nature of the FIFO counters, this register should be read until the same value is returned twice.

### 5.8.16 TXTRG [7:0]: Transmit FIFO Trigger Level - Write-Only

An 8-bit value written to this register sets the TX FIFO trigger level from 0x00 (zero) to 0x40 (64). The TX FIFO trigger level generates an interrupt whenever the data level in the transmit FIFO falls below this preset trigger level.

### 5.8.17 RXCNT[7:0]: Receive FIFO Level Counter - Read-Only

Receive FIFO level byte count from 0x00 (zero) to 0x40 (64). It gives an indication of the number of characters in the receive FIFO. The FIFO level byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data unloading from the receiver FIFO, which reduces CPU bandwidth requirements. Please see the Application Note DAN119 on Exar's website for a detailed discussion of FIFO level counters. Due to the dynamic nature of the FIFO counters, this register should be read until the same value is returned twice.

### 5.8.18 RXTRG[7:0]: Receive FIFO Trigger Level - Write-Only

An 8-bit value written to this register, sets the RX FIFO trigger level from 0x00 (zero) to 0x40 (64). The RX FIFO trigger level generates an interrupt whenever the receive FIFO level rises to this preset trigger level.

The Product (or product) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

**TABLE 20: UART RESET CONDITIONS**

| REGISTERS | RESET STATE |
|---|---|
| DLL | Bits 7-0 = 0xXX |
| DLM | Bits 7-0 = 0xXX |
| RHR | Bits 7-0 = 0xXX |
| THR | Bits 7-0 = 0xXX |
| IER | Bits 7-0 = 0x00 |
| FCR | Bits 7-0 = 0x00 |
| ISR | Bits 7-0 = 0x01 |
| LCR | Bits 7-0 = 0x00 |
| MCR | Bits 7-0 = 0x00 |
| LSR | Bits 7-0 = 0x60 |
| MSR | Bits 3-0 = logic 0<br>Bits 7-4 = logic levels of the inputs |
| SPR | Bits 7-0 = 0xFF |
| FCTR | Bits 7-0 = 0x00 |
| EFR | Bits 7-0 = 0x00 |
| TXCNT | Bits 7-0 = 0x00 |
| TXTRG | Bits 7-0 = 0x00 |
| RXCNT | Bits 7-0 = 0x00 |
| RXTRG | Bits 7-0 = 0x00 |
| XCHAR | Bits 7-0 = 0x00 |
| XON1 | Bits 7-0 = 0x00 |
| XON2 | Bits 7-0 = 0x00 |
| XOFF1 | Bits 7-0 = 0x00 |
| XOFF2 | Bits 7-0 = 0x00 |
| **I/O SIGNALS** | **RESET STATE** |
| TX[ch-3:0] | HIGH (if ENIR pin = LOW)<br>LOW (if ENIR pin = HIGH) |
| RTS#[ch-3:0] | HIGH |
| DTR#[ch-3:0] | HIGH |
| EECK | LOW |
| EECS | LOW |
| EEDI | LOW |

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

# 6.0 PROGRAMMING EXAMPLES

## 6.1 UNLOADING RECEIVE DATA USING THE SPECIAL RECEIVE FIFO DATA WITH STATUS

It is suggested that before starting to read the Special Receive FIFO Data with Status to unload data from any UART channel (address 0x180 for channel 0), do a dummy read to the Device ID (DVID) register in the Configuration Register of the device. The Special Receive FIFO Data with Status register can then be read multiple times subsequently without any byte-swapping problem as long as no other register (except the Device ID register) is accessed in between data unload. If you must read or write to another register, make that dummy read to the DVID register again and continue with data unloading.

A step by step procedure describing the sequence for a target channel is shown below. From the receive data service routine:

- Do a dummy read to Device ID (DVID) register. Address 0x8D in BYTE alignment or address 0x8C in DWORD alignment.
- Read the data byte and its associated error status from 'Special Receive FIFO Data with Status' register of the target channel until done or empty when one of the LSR status byte bit-0=0.

NOTE: If you must do other Read/Write operations to other register(s) during data unloading, repeat steps 1 & 2 to continue unloading data plus status from the 'Special Receive FIFO Data with Status' register of the target channel.

Some Examples of using the Special Receive FIFO Data with Status:

### EXAMPLE I: POLLING

.....
Read LSR
Read DVID
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)*
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
.....

### EXAMPLE 2: INTERRUPT SERVICE USING INTERRUPT INFORMATION IN DEVICE CONFIGURATION REGISTER SET

.....
Read Global Interrupt Register INT0 (address 0x080)
Read INT1 through INT3 registers to identify interrupting channel (address 0x081 through 0x083)
Read DVID
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)*
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
.....

### EXAMPLE 3: INTERRUPT SERVICE USING INTERRUPT INFORMATION IN INDIVIDUAL CHANNEL'S REGISTERS

.....
Read Global Interrupt Register INT0 (address 0x080)
Read ISR register of interrupting channel
Read DVID
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)*
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
.....

* In case some other registers need to be accessed in between 'Special Receive FIFO Data with Status' reads, a 'Read DVID' instruction has to be inserted before resuming 'Special Receive FIFO Data with Status' read operation.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Range (VCC) | 7 volts |
| Voltage at any PCI Bus Pin | -0.5 to (VIO+0.5) volts |
| Voltage at any non-PCI Bus Pin | -0.5 to 7 volts |
| Operating Temperature | -40° to +85° C |
| Storage Temperature | -65° to +150° C |
| Package Dissipation | 500 mW |
| Thermal Resistance (20x20x1.4mm 144-LQFP) | theta-ja = 42, theta-jc = 8 |

## ELECTRICAL CHARACTERISTICS

***DC ELECTRICAL CHARACTERISTICS FOR 5V PCI BUS INTERFACE (VIO = 4.75-5.25V, VCC = 4.5-5.5V)***

***TA=0° to 70°C (-40° to +85°C for industrial grade package).***

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | CONDITION | NOTES |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.8 | V | | All inputs |
| $V_{IH}$ | Input High Voltage | 2.0 | VIO + 0.5 | V | | PCI bus and External Clock inputs |
| $V_{IH}$ | Input High Voltage | 2.0 | 6.0 | V | | Non-PCI bus inputs |
| $V_{OL}$ | Output Low Voltage | | 0.55 | V | Iout=6 mA | All outputs |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | Iout=-2 mA | All outputs |
| $I_{IL}$ | Input Low Leakage Current | | -10 | uA | | |
| $I_{IH}$ | Input High Leakage Current | | 10 | uA | | |
| $I_{CL}$ | Input Clock Leakage | | ±10 | uA | | |
| $C_{IN}$ | Input Pin Capacitance | | 10 | pF | | |
| $C_{CLK}$ | CLK Pin Capacitance | 5 | 12 | pF | | |
| $C_{IDSEL}$ | IDSEL Pin Capacitance | | 8 | pF | | |
| $I_{CC}$ | Power Supply Current | | 4 | mA | PCI Bus CLK and Ext. Clock=2MHz, all inputs are at VCC or GND and all outputs are unloaded | |
| $I_{SLEEP}$ | Sleep Current | | 20 | uA | All four UARTs asleep. AD[31:0] at GND, all inputs at VCC or GND. | **VCC must equal VIO**. See Sleep Mode section on page 19 |

### AC ELECTRICAL CHARACTERISTICS FOR 5V PCI BUS INTERFACE (VIO = 4.75-5.25V, VCC = 4.5-5.5V)

*TA=0° to 70°C (-40° to +85°C for industrial grade package).*

| SYMBOL | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| XTAL1 | UART Crystal Oscillator | | 24 | MHz | |
| ECLK | External Clock | | 50 | MHz | |
| $T_{ECLK}$ | External Clock Period | 20 | | ns | $T_{ECLK}$ = 1/ECLK |
| $T_{ECH}$, $T_{ECL}$ | External Clock High/Low Time | 8 | | ns | |
| $I_{OH(AC)}$ | Switching Current High | -44 | | mA | See PCI Specification Rev. 2.3 |
| $I_{OL(AC)}$ | Switching Current Low | 95 | | mA | See PCI Specification Rev. 2.3 |
| $I_{CL}$ | Low Clamp Current | -25+(Vin+1)/0.015 | | mA | -5 < Vin ≤ -1 |
| $Slew_R$ | Output Rise Slew Rate | 1 | 4 | V/ns | 0.4V to 2.4V load |
| $Slew_F$ | Output Fall Slew Rate | 1 | 4 | V/ns | 2.4V to 0.4V load |
| $T_{CYC}$ | CLK Cycle Time | 30 | ∞ | ns | PCI Bus Clock, CLK |
| $T_{HI}$ | CLK High Time | 11 | | ns | |
| $T_{LO}$ | CLK Low Time | 11 | | ns | |
| | CLK Slew Rate | 1 | 4 | V/ns | |
| $T_{VAL}$ | CLK to Signal Valid Delay | 2 | 11 | ns | |
| $T_{ON}$ | Float to Active Delay | 2 | | ns | |
| $T_{OFF}$ | Active to Float Delay | | 28 | ns | |
| $T_{SETUP}$ | Input Setup Time to CLK - bused signals | 7 | | ns | |
| $T_{HOLD}$ | Input Hold Time from CLK | 0 | | ns | |
| | | | | | |
| $T_{PRST}$ | RST# Active Time After Power Stable | 1 | | ms | |
| $T_{CRST\#}$ | RST# Active Time After CLK Stable | 100 | | us | |
| | RST# Slew Rate | 50 | | mV/ns | |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### DC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 3.0-5.5V)

*TA=0° to 70°C (-40° to +85°C for industrial grade package).*

| SYMBOL | PARAMETER | MIN | MAX | UNITS | CONDITION | NOTES |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.3VIO | V | | For PCI bus inputs |
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.8 | V | | For Non-PCI bus inputs |

## DC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 3.0-5.5V)

*TA=0° to 70°C (-40° to +85°C for industrial grade package).*

| SYMBOL | PARAMETER | MIN | MAX | UNITS | CONDITION | NOTES |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 0.5VIO | VIO + 0.5 | | | For PCI bus and external clock inputs |
| $V_{IH}$ | Input High Voltage | 2.0 | 6 | V | | For non-PCI bus inputs |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 4mA | All outputs |
| $V_{OH}$ | Output High Voltage | 0.9VIO | | V | $I_{OH}$ = -0.5mA | PCI bus outputs |
| $V_{OH}$ | Output High Voltage | 2.0 | | V | $I_{OH}$ = -1mA VCC = 3.0 - 3.6V | Non-PCI bus outputs |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = -2mA VCC = 4.5 - 5.5V | Non-PCI bus outputs |
| $I_{IL}$ | Input Low Leakage Current | | -10 | µA | | |
| $I_{IH}$ | Input High Leakage Current | | 10 | µA | | |
| $I_{CL}$ | Input Clock Leakage | | ±10 | µA | | |
| $C_{IN}$ | Input Pin Capacitance | | 10 | pF | | |
| $C_{CLK}$ | CLK Pin Capacitance | 5 | 12 | pF | | |
| $C_{IDSEL}$ | IDSEL Pin Capacitance | | 8 | pF | | |
| $I_{CC}$ | Power Supply Current | | 2 | mA | PCI Bus CLK and Ext. Clock=2MHz, all inputs are at VCC or GND and all outputs are unloaded | |
| $I_{SLEEP}$ | Sleep Current | | 20 | µA | All four UARTs asleep. AD[31:0] at GND, all inputs at VCC or GND | **VCC must equal VIO**. See Sleep Mode section on page 19 |

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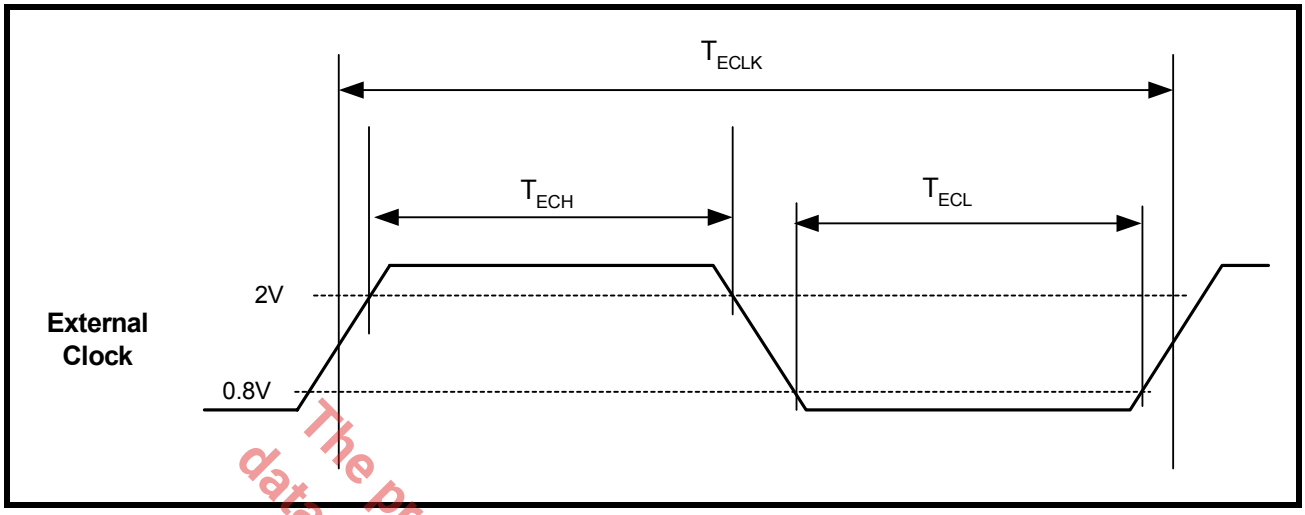
## *AC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 3.0-5.5V)*

***TA=0° to 70°C (-40° to +85°C for industrial grade package).***

| SYMBOL | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| XTAL1 | UART Crystal Oscillator | | 24 | MHz | On-chip osc. |
| ECLK | External Clock | | 33 | MHz | VCC = 3.3V ±10% |
| | | | 50 | MHz | VCC = 5V ±10% |
| $T_{ECLK}$ | External Clock Period ($T_{ECLK}$ = 1/ECLK) | 30 | | ns | VCC = 3.3V ±10% |
| | | 20 | | ns | VCC = 5V ±10% |
| $T_{ECH}$, $T_{ECL}$ | External Clock High/Low Time | 13 | | ns | VCC = 3.3V ±10% |
| | | 8 | | ns | VCC = 5V ±10% |
| $I_{OH(AC)}$ | Switching Current High | -12VIO | | mA | See PCI Specification Rev. 2.3 |
| $I_{OL(AC)}$ | Switching Current Low | 16VIO | | mA | See PCI Specification Rev. 2.3 |
| $I_{CH}$ | High Clamp Current | 25+(Vin-VIO-1)/0.015 | | mA | VIO+4 > Vin ≥ VIO+1 |
| $I_{CL}$ | Low Clamp Current | -25+(Vin+1)/0.015 | | mA | -3 < Vin ≤ -1 |
| $Slew_R$ | Output Rise Slew Rate | 1 | 4 | V/ns | 0.2VIO - 0.6VIO load |
| $Slew_F$ | Output Fall Slew Rate | 1 | 4 | V/ns | 0.6VIO - 0.2VIO load |
| $T_{CYC}$ | CLK Cycle Time | 30 | ∞ | ns | PCI Bus Clock, CLK |
| $T_{HI}$ | CLK High Time | 11 | | ns | |
| $T_{LO}$ | CLK Low Time | 11 | | ns | |
| | CLK Slew Rate | 1 | 4 | V/ns | |
| $T_{VAL}$ | CLK to Signal Valid Delay | 2 | 11 | ns | |
| $T_{ON}$ | Float to Active Delay | 2 | | ns | |
| $T_{OFF}$ | Active to Float Delay | | 28 | ns | |
| $T_{SETUP}$ | Input Setup Time to CLK - bused signals | 7 | | ns | |
| $T_{HOLD}$ | Input Hold Time from CLK | 0 | | ns | |
| $T_{PRST}$ | RST# Active Time After Power Stable | 1 | | ms | |
| $T_{CRST\#}$ | RST# Active Time After CLK Stable | 100 | | us | |
| | RST# Slew Rate | 50 | | mV/ns | |

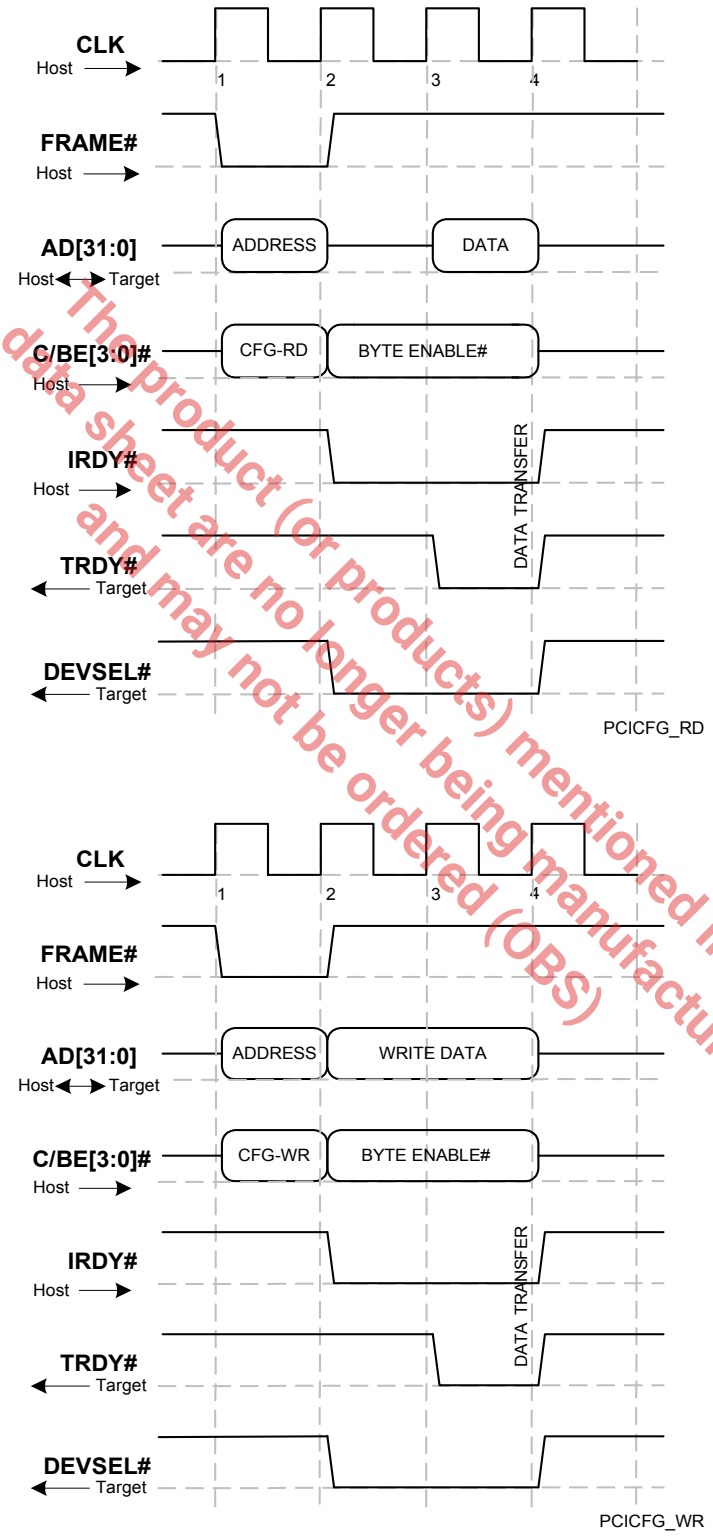
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FIGURE 19. TIMING FOR EXTERNAL CLOCK INPUT AT XTAL1 PIN



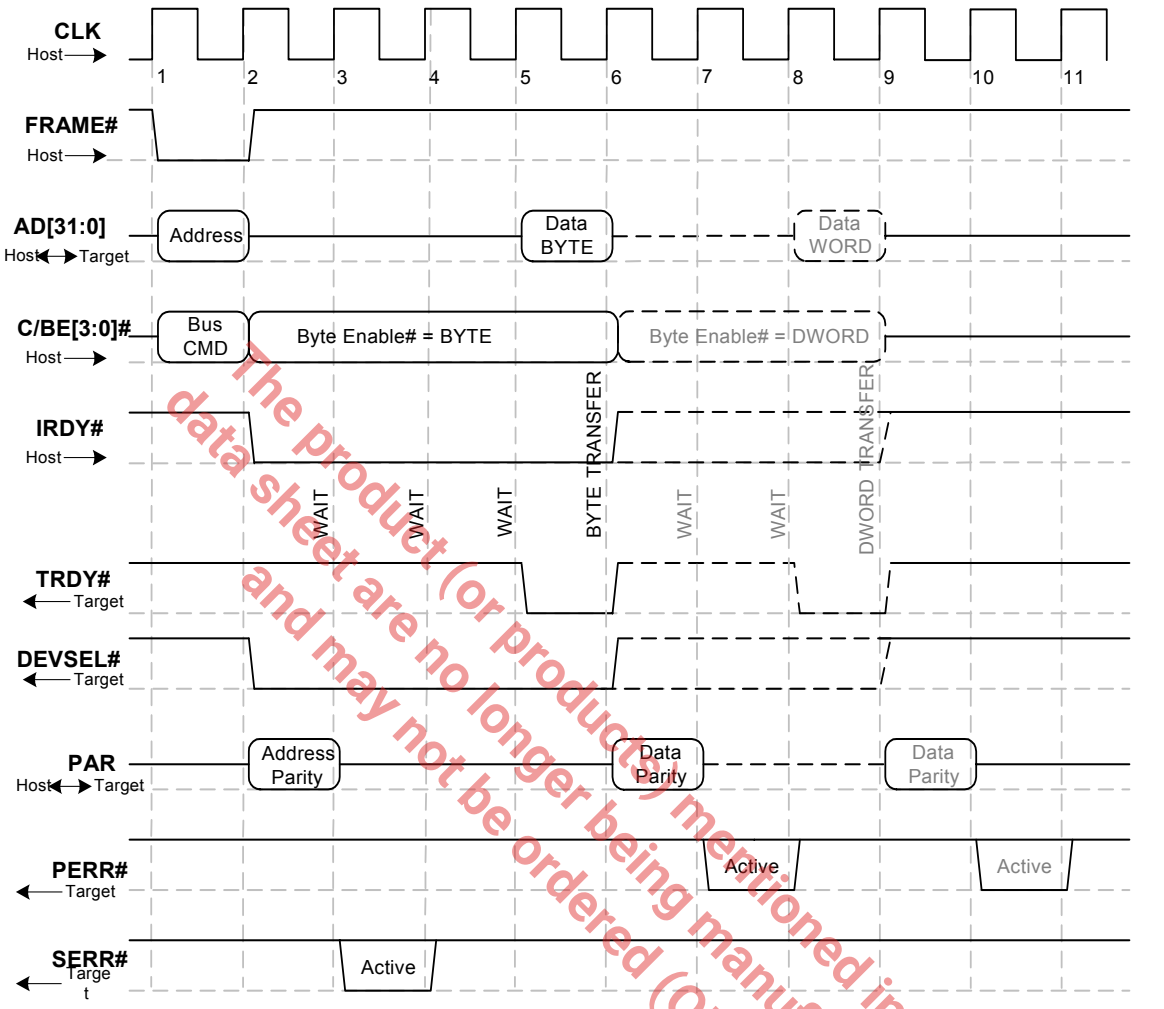

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FIGURE 20. PCI BUS CONFIGURATION SPACE REGISTERS READ AND WRITE OPERATION




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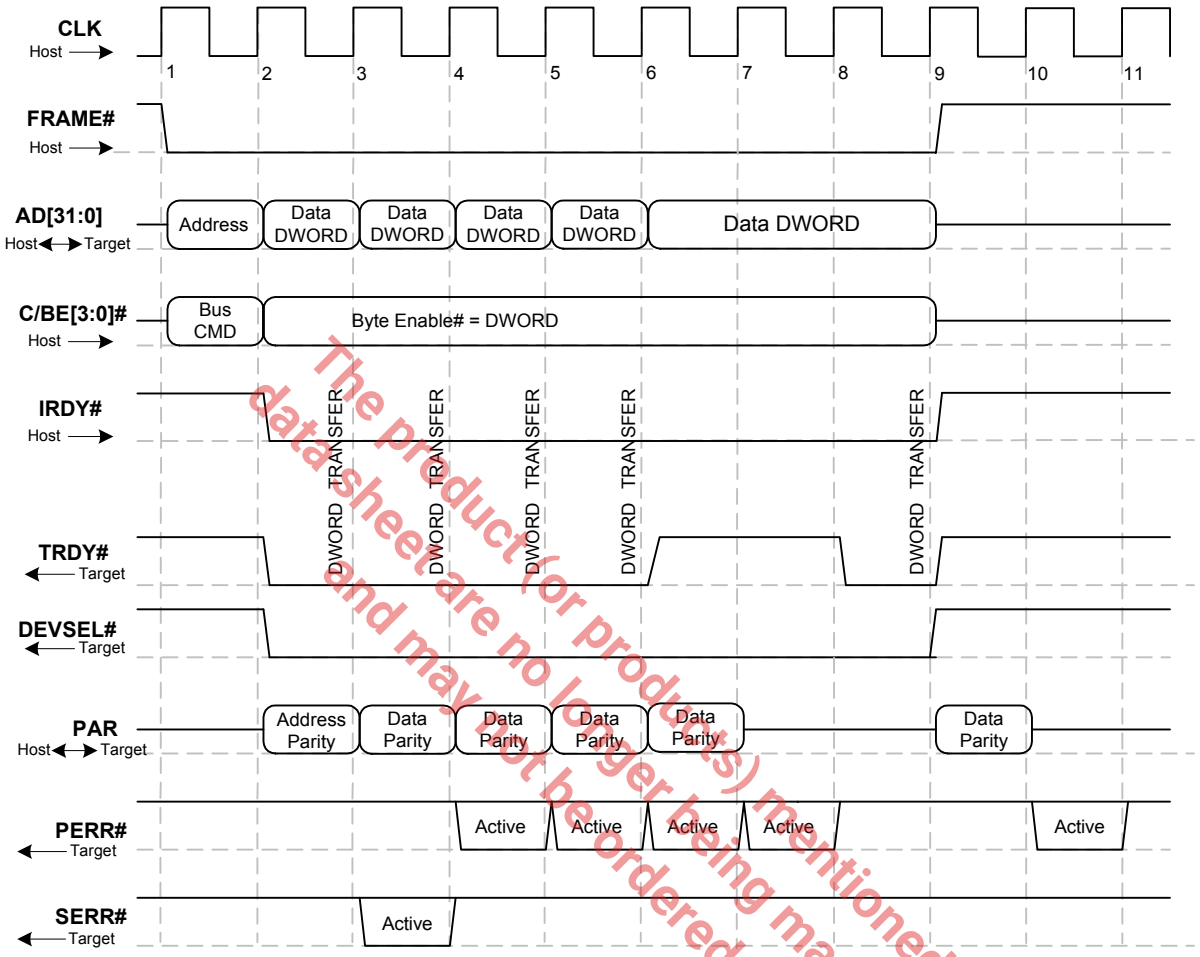
FIGURE 21. DEVICE CONFIGURATION AND UART REGISTERS READ OPERATION FOR A BYTE OR DWORD




Note: PERR# and SERR are optional in a bus target application.
Even Parity is on AD[31:0], C/BE[3:0]#, and PAR

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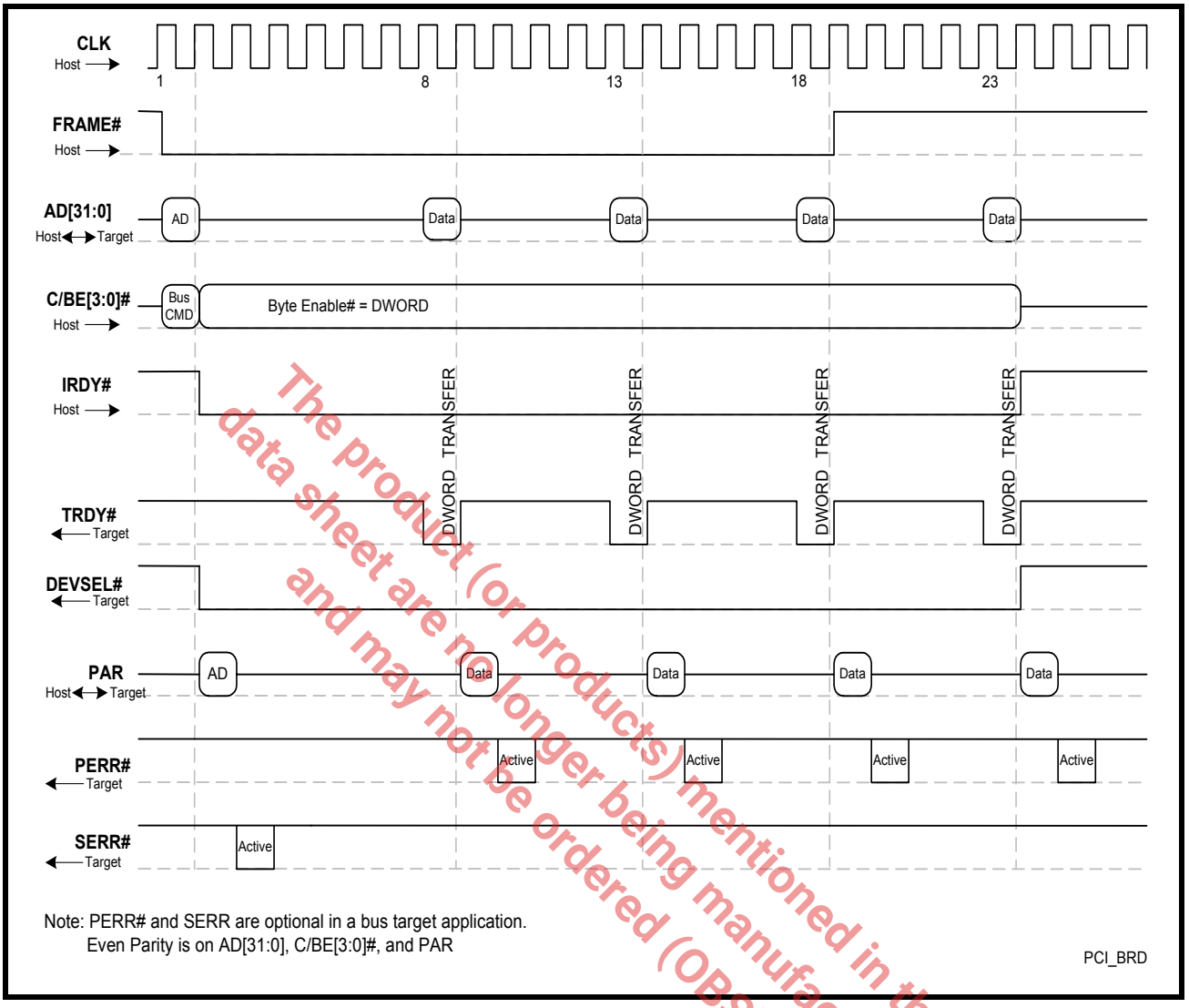
FIGURE 22. DEVICE CONFIGURATION REGISTERS, UART REGISTERS AND TRANSMIT DATA BURST WRITE OPERATION




Note: PERR# and SERR are optional in a bus target application.
Even Parity is on AD[31:0], C/BE[3:0]#, and PAR

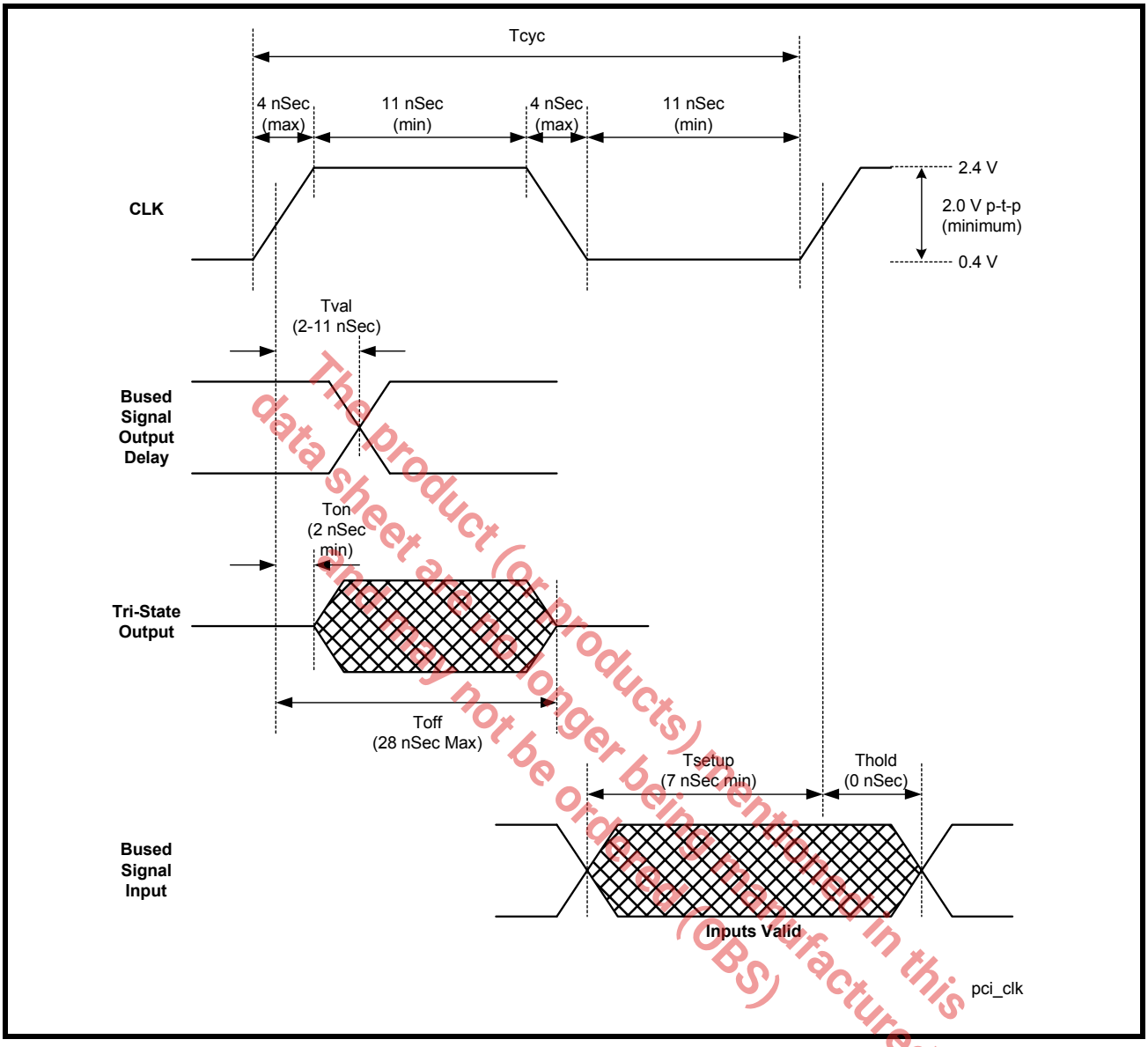
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FIGURE 23. DEVICE CONFIGURATION REGISTERS, UART REGISTERS AND RECEIVE DATA BURST READ OPERATION



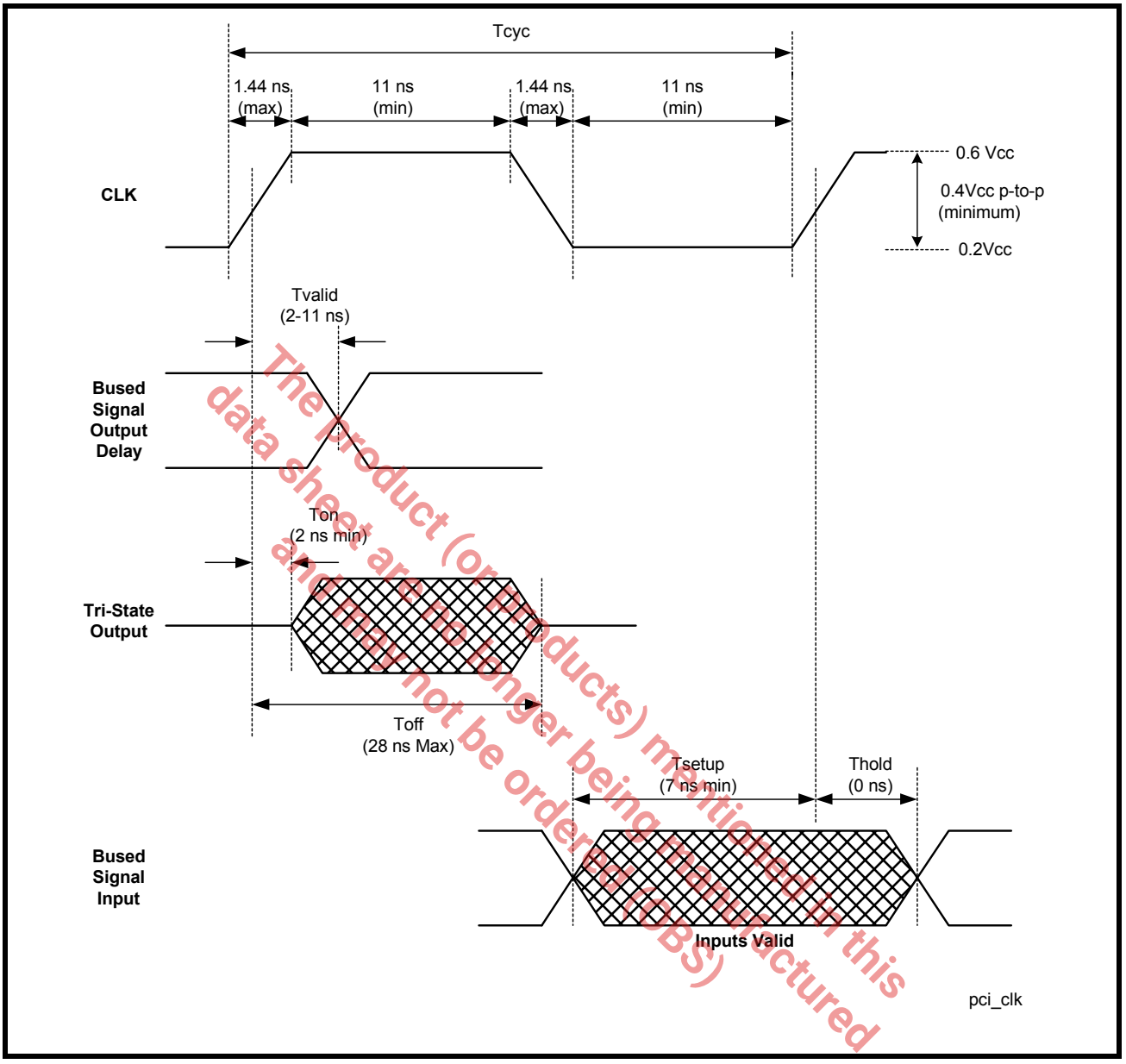

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FIGURE 24. 5V PCI BUS CLOCK (DC TO 33MHZ)




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FIGURE 25. 3.3V PCI BUS CLOCK (DC TO 33MHZ)




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**FIGURE 26. TRANSMIT DATA INTERRUPT AT TRIGGER LEVEL**

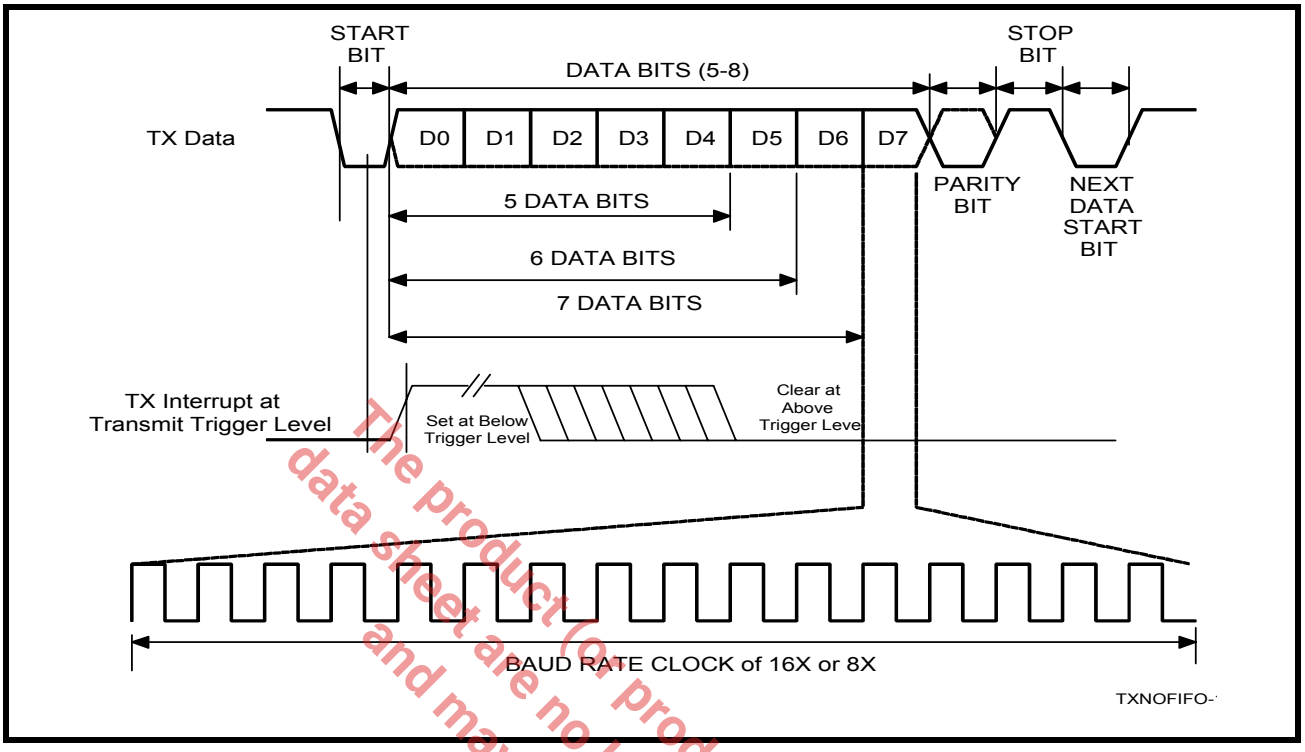
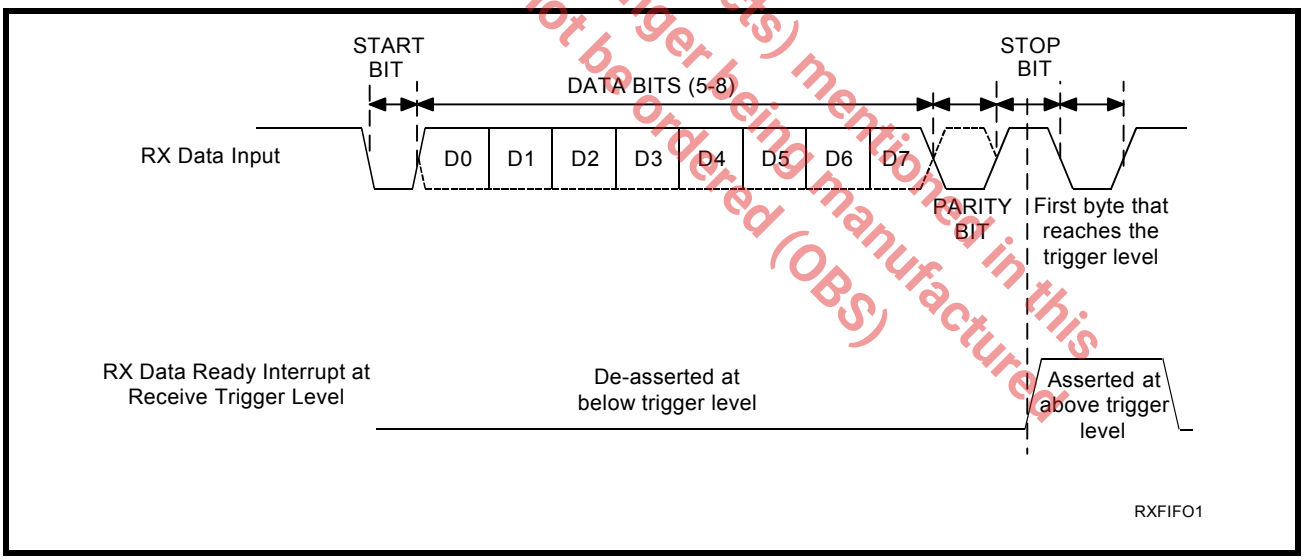


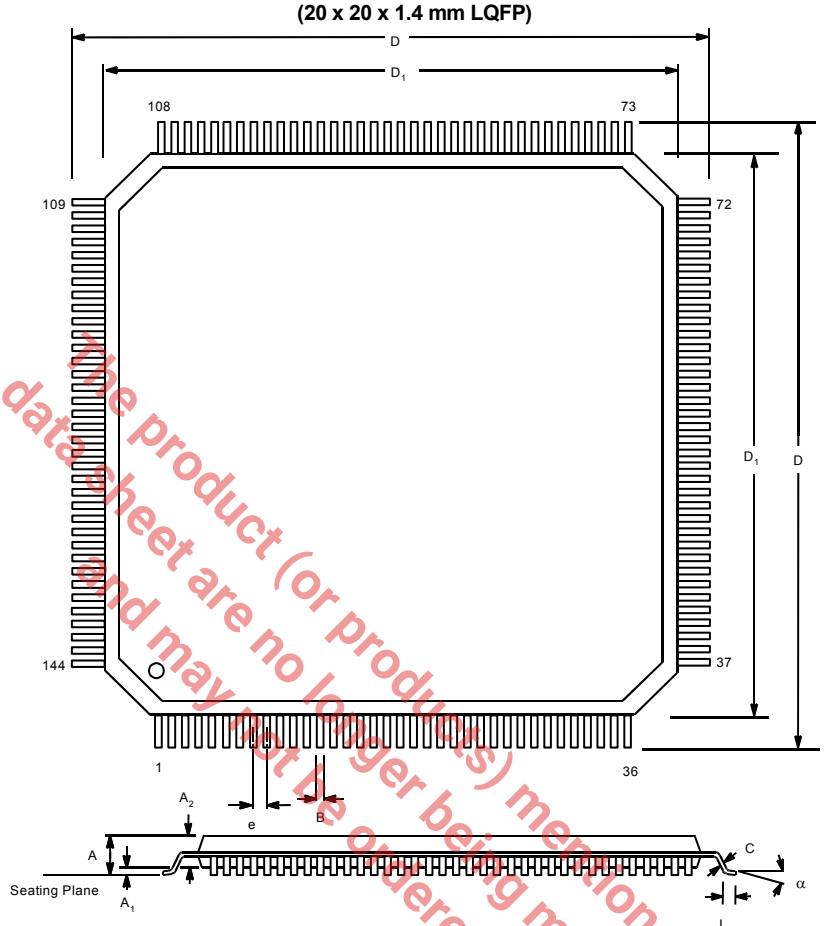

**FIGURE 27. RECEIVE DATA READY INTERRUPT AT TRIGGER LEVEL**




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## PACKAGE DIMENSIONS

144 LEAD LOW-PROFILE QUAD FLAT PACK
(20 x 20 x 1.4 mm LQFP)




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**NOTE:** *Note: The control dimension is the millimeter column*

| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.055 | 0.063 | 1.40 | 1.60 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.053 | 0.057 | 1.35 | 1.45 |
| B | 0.007 | 0.011 | 0.17 | 0.27 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.858 | 0.874 | 21.80 | 22.20 |
| D1 | 0.783 | 0.791 | 19.90 | 20.10 |
| e | 0.020 BSC | | 0.50 BSC | |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| α | 0× | 7× | 0× | 7× |

## REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| May 2003 | Rev. 1.0.0 | Final Production Release. Clarified the DC and AC Electrical Characteristics. Updated requirements for Sleep Mode. |
| July 2003 | Rev 1.1.0 | Added Device Status to Ordering Information. |
| June 2004 | Rev 1.2.0 | Clarified pin descriptions- changed from using logic 1 and logic 0 to HIGH (VCC) and LOW (GND) for input and output pin descriptions. Clarified Auto RS485 and Sleep Mode description. Added timing diagram for external clock input at XTAL1 pin (**Figure 19**) and $T_{ECLK}$, $T_{ECH}$, and $T_{ECL}$ to AC Electrical Specifications. The Device Revision Register (DREV) has been updated to 0x02 for devices with top mark date code "B2 YYWW". |
| November 2004 | Rev 1.2.1 | The Device Revision Register (DREV) has been updated to 0x04 for devices with top mark date code "D2 YYWW". |
| August 2005 | Rev 1.2.2 | Updated the 1.4mm-thick Quad Flat Pack package description from "TQFP" to "LQFP" to be consistent with JEDEC and Industry norms. |

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# TABLE OF CONTENTS

GENERAL DESCRIPTION ..... 1
APPLICATIONS ..... 1
FEATURES ..... 1
FIGURE 1. BLOCK DIAGRAM ..... 1
ORDERING INFORMATION ..... 2
FIGURE 2. PIN OUT OF THE DEVICE ..... 2
PIN DESCRIPTIONS ..... 3
PCI LOCAL BUS INTERFACE ..... 3
MODEM OR SERIAL I/O INTERFACE ..... 3
ANCILLARY SIGNALS ..... 4
FUNCTIONAL DESCRIPTION ..... 7
PCI Local Bus Interface ..... 7
PCI Local Bus Configuration Space Registers ..... 7
EEPROM Interface ..... 7
1.0 APPLICATION EXAMPLES ..... 8
TABLE 1: VALID COMBINATIONS OF VCC AND VIO SUPPLY VOLTAGES ..... 8
FIGURE 3. TYPICAL APPLICATION FOR A UNIVERSAL ADD-IN CARD ..... 8
FIGURE 4. TYPICAL APPLICATIONS IN AN EMBEDDED SYSTEM ..... 9
2.0 XR17D154 REGISTERS ..... 10
FIGURE 5. THE XR17D154 REGISTER SETS ..... 10
2.1 PCI LOCAL BUS CONFIGURATION SPACE REGISTERS ..... 10
TABLE 2: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS ..... 11
2.2 DEVICE CONFIGURATION REGISTER SET ..... 12
TABLE 3: XR17D154 DEVICE CONFIGURATION REGISTERS ..... 13
TABLE 4: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT ..... 14
TABLE 5: DEVICE CONFIGURATION REGISTERS SHOWN IN DWORD ALIGNMENT ..... 14
2.2.1 THE INTERRUPT STATUS REGISTER ..... 15
FIGURE 6. THE GLOBAL INTERRUPT REGISTER, INT0, INT1, INT2 AND INT3 ..... 16
TABLE 6: UART CHANNEL [3:0] INTERRUPT SOURCE ENCODING ..... 16
TABLE 7: UART CHANNEL [3:0] INTERRUPT CLEARING: ..... 17
2.2.2 GENERAL PURPOSE 16-BIT TIMER/COUNTER [TIMERMSB, TIMERLSB, TIMER, TIMECNTL] (DEFAULT 0XXX-XX-00-00) ..... 17
FIGURE 7. TIMER/COUNTER CIRCUIT ..... 17
TABLE 8: TIMER CONTROL REGISTERS ..... 17
2.2.3 8XMODE [7:0] - (DEFAULT 0X00) ..... 18
2.2.4 REGA [15:8] RESERVED ..... 18
2.2.5 RESET [23:16] - (DEFAULT 0X00) ..... 18
2.2.6 SLEEP [31:24] - (DEFAULT 0X00) ..... 19
2.2.7 DEVICE IDENTIFICATION AND REVISION ..... 20
2.2.8 REGB REGISTER ..... 20
2.2.9 MULTI-PURPOSE INPUTS AND OUTPUTS ..... 20
2.2.10 MPIO REGISTER ..... 21
FIGURE 8. MULTIPURPOSE INPUT/OUTPUT INTERNAL CIRCUIT ..... 21
3.0 CRYSTAL OSCILLATOR / BUFFER ..... 23
FIGURE 9. TYPICAL OSCILLATOR CONNECTIONS ..... 23
FIGURE 10. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE ..... 23
4.0 TRANSMIT AND RECEIVE DATA ..... 24
4.1 DATA LOADING AND UNLOADING VIA 32-BIT PCI BURST TRANSFERS ..... 24
4.1.1 NORMAL RX FIFO DATA UNLOADING AT LOCATIONS 0X100, 0X300, 0X500, 0X700 ..... 24
4.1.2 SPECIAL RX FIFO DATA UNLOADING AT LOCATIONS 0X180, 0X380, 0X580, AND 0X780 ..... 25
4.1.3 TX FIFO DATA LOADING AT LOCATIONS 0X100, 0X300, 0X500, 0X700 ..... 26
4.2 FIFO DATA LOADING AND UNLOADING THROUGH THE UART CHANNEL REGISTERS, THR AND RHR IN 8-BIT FORMAT ..... 26
TABLE 9: TRANSMIT AND RECEIVE DATA REGISTER IN BYTE FORMAT, 16C550 COMPATIBLE ..... 26
5.0 UART ..... 27
5.1 PROGRAMMABLE BAUD RATE GENERATOR ..... 27
FIGURE 11. BAUD RATE GENERATOR ..... 27
TABLE 10: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING ..... 28
5.2 TRANSMITTER ..... 28

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5.2.1 TRANSMIT HOLDING REGISTER (THR) - WRITE-ONLY ..... 28
5.2.2 TRANSMITTER OPERATION IN NON-FIFO MODE ..... 28
FIGURE 12. TRANSMITTER OPERATION IN NON-FIFO MODE ..... 29
5.2.3 TRANSMITTER OPERATION IN FIFO MODE ..... 29
5.2.4 AUTO RS485 OPERATION ..... 29
FIGURE 13. TRANSMIITTER OPERATION IN FIFO AND FLOW CONTROL MODE ..... 29
5.3 RECEIVER ..... 30
5.3.1 RECEIVE HOLDING REGISTER (RHR) - READ-ONLY ..... 30
5.3.2 RECEIVER OPERATION IN NON-FIFO MODE ..... 30
FIGURE 14. RECEIVER OPERATION IN NON-FIFO MODE ..... 30
5.3.3 RECEIVER OPERATION WITH FIFO ..... 31
FIGURE 15. RECEIVER OPERATION IN FIFO AND FLOW CONTROL MODE ..... 31
5.4 AUTOMATIC HARDWARE (RTS/CTS OR DTR/DSR) FLOW CONTROL OPERATION ..... 31
TABLE 11: AUTO RTS/CTS OR DTR/DSR FLOW CONTROL SELECTION ..... 31
FIGURE 16. AUTO RTS/DTR AND CTS/DSR FLOW CONTROL OPERATION ..... 32
5.5 INFRARED MODE ..... 33
FIGURE 17. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING ..... 33
5.6 INTERNAL LOOPBACK ..... 34
FIGURE 18. INTERNAL LOOP BACK ..... 34
5.7 UART CHANNEL CONFIGURATION REGISTERS AND ADDRESS DECODING ..... 34
TABLE 12: UART CHANNEL CONFIGURATION REGISTERS ..... 35
TABLE 13: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED BY EFR BIT-4. ..... 36
5.8 REGISTERS ..... 37
5.8.1 RECEIVE HOLDING REGISTER (RHR) - READ-ONLY ..... 37
5.8.2 TRANSMIT HOLDING REGISTER (THR) - WRITE-ONLY ..... 37
5.8.3 BAUD RATE GENERATOR DIVISORS (DLL AND DLM) - READ/WRITE ..... 37
5.8.4 INTERRUPT ENABLE REGISTER (IER) - READ/WRITE ..... 37
IER versus Receive FIFO Interrupt Mode Operation ..... 37
IER versus Receive/Transmit FIFO Polled Mode Operation ..... 37
5.8.5 INTERRUPT STATUS REGISTER (ISR) - READ-ONLY ..... 38
TABLE 14: INTERRUPT SOURCE AND PRIORITY LEVEL ..... 39
5.8.6 FIFO CONTROL REGISTER (FCR) - WRITE-ONLY ..... 40
TABLE 15: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION ..... 41
5.8.7 LINE CONTROL REGISTER (LCR) - READ/WRITE ..... 42
TABLE 16: PARITY SELECTION ..... 43
5.8.8 MODEM CONTROL REGISTER (MCR) - READ/WRITE ..... 43
5.8.9 LINE STATUS REGISTER (LSR) - READ/ONLY ..... 44
5.8.10 MODEM STATUS REGISTER (MSR) - READ-ONLY ..... 45
5.8.11 MODEM STATUS REGISTER (MSR) - WRITE-ONLY ..... 46
TABLE 17: AUTO RS485 HALF-DUPLEX DIRECTION CONTROL DELAY FROM TRANSMIT-TO-RECEIVE ..... 46
5.8.12 SCRATCH PAD REGISTER (SPR) - READ/WRITE ..... 47
5.8.13 FEATURE CONTROL REGISTER (FCTR) - READ/WRITE ..... 47
TABLE 18: 16 SELECTABLE HYSTERESIS LEVELS WHEN TRIGGER TABLE-D IS SELECTED ..... 48
5.8.14 ENHANCED FEATURE REGISTER (EFR) - READ/WRITE ..... 48
TABLE 19: SOFTWARE FLOW CONTROL FUNCTIONS ..... 49
5.8.15 TXCNT[7:0]: TRANSMIT FIFO LEVEL COUNTER - READ-ONLY ..... 50
5.8.16 TXTRG [7:0]: TRANSMIT FIFO TRIGGER LEVEL - WRITE-ONLY ..... 50
5.8.17 RXCNT[7:0]: RECEIVE FIFO LEVEL COUNTER - READ-ONLY ..... 50
5.8.18 RXTRG[7:0]: RECEIVE FIFO TRIGGER LEVEL - WRITE-ONLY ..... 50
TABLE 20: UART RESET CONDITIONS ..... 51
6.0 PROGRAMMING EXAMPLES ..... 52
6.1 UNLOADING RECEIVE DATA USING THE SPECIAL RECEIVE FIFO DATA WITH STATUS ..... 52
ABSOLUTE MAXIMUM RATINGS ..... 53
ELECTRICAL CHARACTERISTICS ..... 53
*DC ELECTRICAL CHARACTERISTICS FOR 5V PCI BUS INTERFACE (VIO = 4.75-5.25V, VCC = 4.5-5.5V) 53*
*AC ELECTRICAL CHARACTERISTICS FOR 5V PCI BUS INTERFACE (VIO = 4.75-5.25V, VCC = 4.5-5.5V) 54*
*DC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 3.0-5.5V) 54*
*AC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 3.0-5.5V) 56*
FIGURE 19. TIMING FOR EXTERNAL CLOCK INPUT AT XTAL1 PIN ..... 57
FIGURE 20. PCI BUS CONFIGURATION SPACE REGISTERS READ AND WRITE OPERATION ..... 58
FIGURE 21. DEVICE CONFIGURATION AND UART REGISTERS READ OPERATION FOR A BYTE OR DWORD ..... 59

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FIGURE 22. DEVICE CONFIGURATION REGISTERS, UART REGISTERS AND TRANSMIT DATA BURST WRITE OPERATION ..... 60
FIGURE 23. DEVICE CONFIGURATION REGISTERS, UART REGISTERS AND RECEIVE DATA BURST READ OPERATION ..... 61
FIGURE 24. 5V PCI BUS CLOCK (DC TO 33MHZ) ..... 62
FIGURE 25. 3.3V PCI BUS CLOCK (DC TO 33MHZ) ..... 63
FIGURE 26. TRANSMIT DATA INTERRUPT AT TRIGGER LEVEL ..... 64
FIGURE 27. RECEIVE DATA READY INTERRUPT AT TRIGGER LEVEL ..... 64
**PACKAGE DIMENSIONS ..... 65**
REVISION HISTORY ..... 66
***TABLE OF CONTENTS ..... I***

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)