## GENERAL DESCRIPTION

The XRA1403 is an 16-bit GPIO expander with an SPI interface. After power-up, the XRA1403 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the XRA1403 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The XRA1403 is available in 24-pin QFN and 24-pin TSSOP packages.

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The product(s) mentioned in this

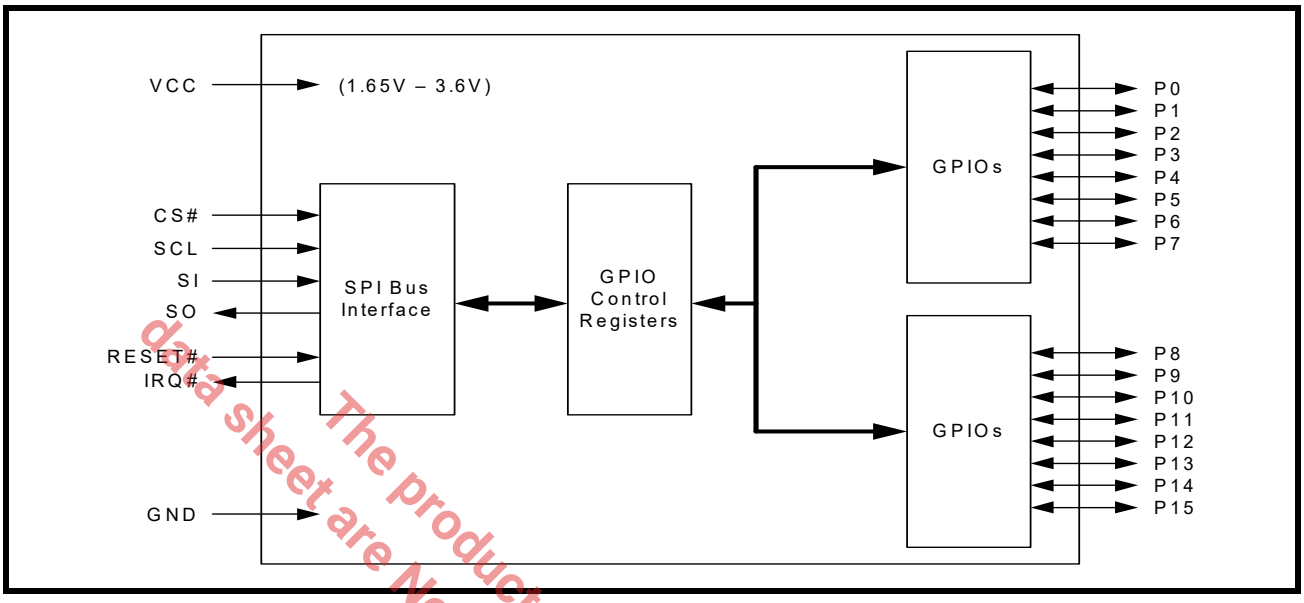
### *FEATURES*

- 1.65V to 3.6V operating voltage
- 16 General Purpose I/Os (GPIOs)
- 5V tolerant inputs
- Maximum stand-by current of 1uA at +1.8V
- SPI bus interface
  - SPI Clock Frequency up to 26MHz
- Individually programmable inputs
  - Internal pull-up resistors
  - Polarity inversion
  - Individual interrupt enable
  - Rising edge and/or Falling edge interrupt
  - Input filter
- Individually programmable outputs
  - Output Level Control
  - Output Three-State Control
- Open-drain active low interrupt output
- Active-low reset input
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

### *APPLICATIONS*

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

**FIGURE 1. XRA1403 BLOCK DIAGRAM**




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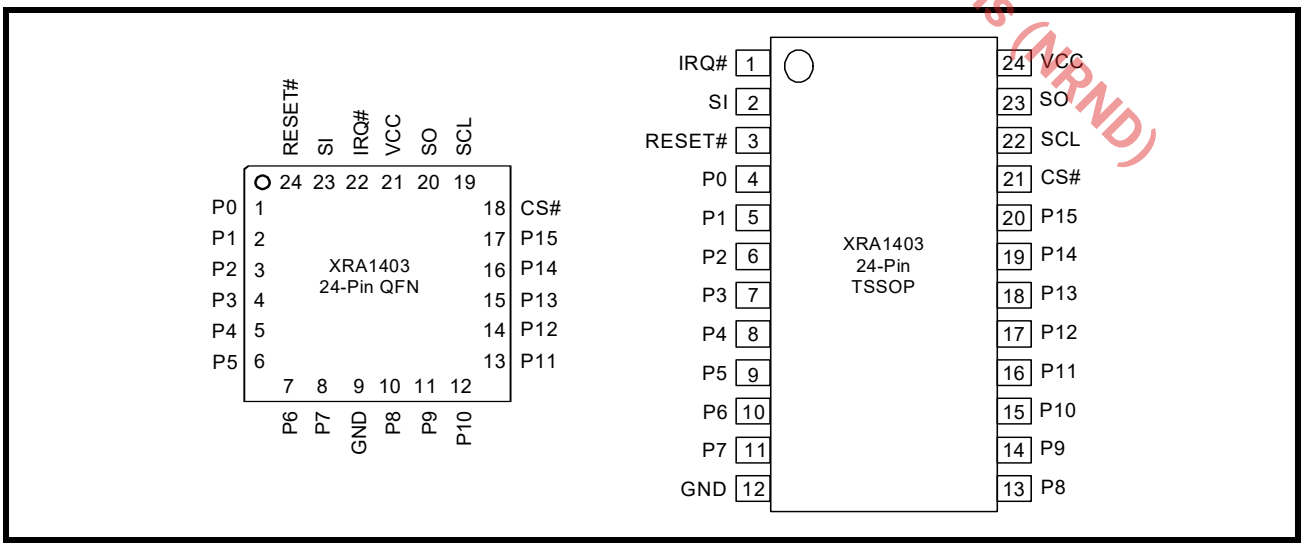
## *ORDERING INFORMATION*[1]

| PART NUMBER | NUMBER OF GPIOS | OPERATING TEMPERATURE RANGE | PACKAGE | PACKAGE METHOD | LEAD FREE[2] |
|---|---|---|---|---|---|
| XRA1403IL24-F | 16 | -40°C to +85°C | QFN-24 | Tray | Yes |
| XRA1403IL24TR-F | 16 | -40°C to +85°C | QFN-24 | Tape and Reel | Yes |
| XRA1403IG24TR-F | 16 | -40°C to +85°C | TSSOP-24 | Tape and Reel | Yes |
| XRA1403IL24-0B-EB | XRA1403 24-pin QFN Evaluation Board | | | | |
| XRA1403IG24-0B-EB | XRA1403 24-pin TSSOP Evaluation Board | | | | |

***NOTES:***

1. *Refer to www.maxlinear.com/XRA1403 for most up-to-date Ordering Information.*
2. *Visit www.maxlinear.com for additional information on Environmental Rating.*

**FIGURE 2. PIN OUT ASSIGNMENTS**



# PIN DESCRIPTIONS

## Pin Description

| NAME | QFN-24 PIN# | TSSOP-24 PIN# | TYPE | DESCRIPTION |
|---|---|---|---|---|
| **SPI INTERFACE** | | | | |
| SO | 20 | 23 | O | SPI serial data output. |
| SCL | 19 | 22 | I | SPI bus serial input clock. |
| IRQ# | 22 | 1 | OD | Interrupt output (open-drain, active LOW). |
| CS# | 18 | 21 | I | SPI bus chip select. |
| SI | 23 | 2 | I | SPI serial data input. |
| RESET# | 24 | 3 | I | Reset (active LOW) - A longer than 40 ns LOW pulse on this pin will reset the internal registers and all GPIOs will be configured as inputs. |
| **GPIOs** | | | | |
| P0 | 1 | 4 | I/O | General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up or after a reset. |
| P1 | 2 | 5 | I/O | |
| P2 | 3 | 6 | I/O | |
| P3 | 4 | 7 | I/O | |
| P4 | 5 | 8 | I/O | |
| P5 | 6 | 9 | I/O | |
| P6 | 7 | 10 | I/O | |
| P7 | 8 | 11 | I/O | |
| P8 | 10 | 13 | I/O | General purpose I/O P8-P15. All GPIOs are configured as inputs upon power-up or after a reset. |
| P9 | 11 | 14 | I/O | |
| P10 | 12 | 15 | I/O | |
| P11 | 13 | 16 | I/O | |
| P12 | 14 | 17 | I/O | |
| P13 | 15 | 18 | I/O | |
| P14 | 16 | 19 | I/O | |
| P15 | 17 | 20 | I/O | |
| **ANCILLARY SIGNALS** | | | | |
| VCC | 21 | 24 | Pwr | 1.65V to 3.6V VCC supply voltage. |
| GND | 9 | 12 | Pwr | Power supply common, ground. |
| GND | Center Pad | - | Pwr | The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential. |

**Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.**

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## 1.0 FUNCTIONAL DESCRIPTION

### *1.1 SPI bus Interface*

The SPI interface consists of four lines: serial clock (SCL), chip select (CS#), slave output (SO) and slave input (SI). The serial clock, slave output and slave input can be as fast as 26 MHz. To access the device in the SPI mode, the CS# signal is asserted by the SPI master, then the SPI master starts toggling the SCL signal with the appropriate transaction information. The first bit sent by the SPI master includes whether it is a read or write transaction and the register being accessed. See Table 1 below.

**TABLE 1: SPI COMMAND BYTE FORMAT**

| BIT | FUNCTION |
|---|---|
| 7 | Read/Write#<br>Logic 1 = Read<br>Logic 0 = Write |
| 6:1 | Command Byte |
| 0 | Reserved |

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**FIGURE 3. SPI WRITE**

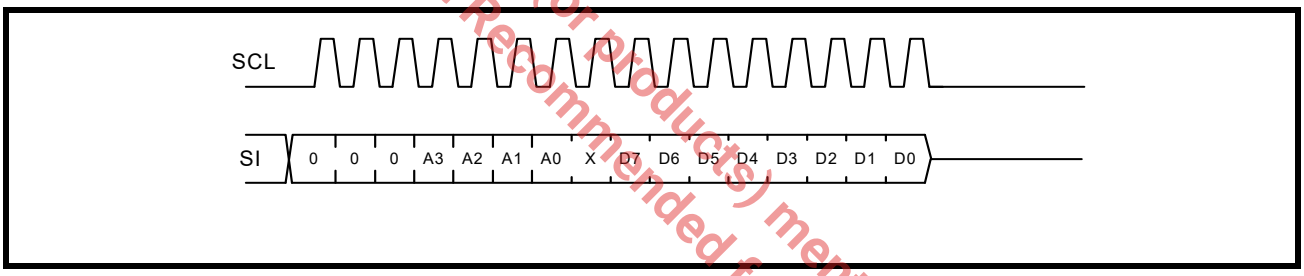
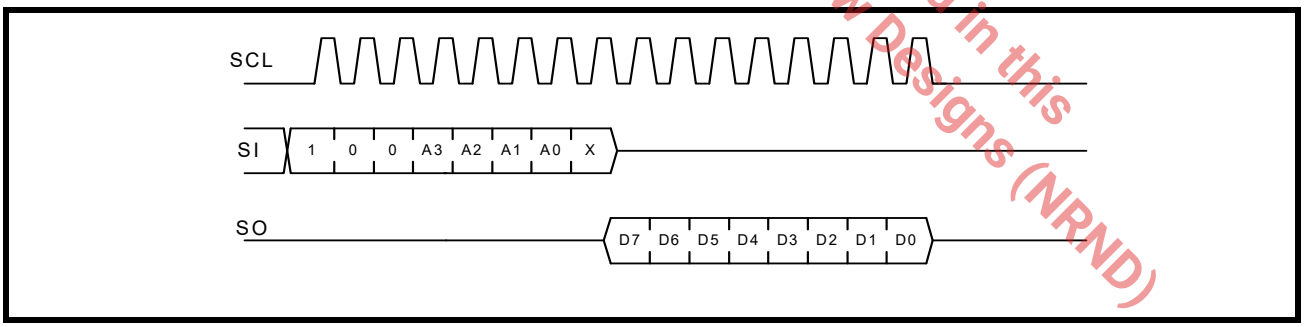



**FIGURE 4. SPI READ**




After the last read or write transaction, the SPI master will set the SCL signal back to its idle state (LOW).

### 1.1.1 SPI Command Byte

An SPI command byte is sent by the SPI master following the slave address. The command byte indicates the address offset of the register that will be accessed. Table 2 below lists the command bytes for each register.

**TABLE 2: COMMAND BYTE (REGISTER ADDRESS)**

| COMMAND BYTE | REGISTER NAME DESCRIPTION | READ/WRITE | DEFAULT VALUES |
|---|---|---|---|
| 0x00 | GSR1 - GPIO State for P0-P7 | Read-Only | 0xXX |
| 0x01 | GSR2 - GPIO State for P8-P15 | Read-Only | 0xXX |
| 0x02 | OCR1 - Output Control for P0-P7 | Read/Write | 0xFF |
| 0x03 | OCR2 - Output Control for P8-P15 | Read/Write | 0xFF |
| 0x04 | PIR1 - Input Polarity Inversion for P0-P7 | Read/Write | 0x00 |
| 0x05 | PIR2 - Input Polarity Inversion for P8-P15 | Read/Write | 0x00 |
| 0x06 | GCR1 - GPIO Configuration for P0-P7 | Read/Write | 0xFF |
| 0x07 | GCR2 - GPIO Configuration for P8-P15 | Read/Write | 0xFF |
| 0x08 | PUR1 - Input Internal Pull-up Resistor Enable/Disable for P0-P7 | Read/Write | 0x00 |
| 0x09 | PUR2 - Input Internal Pull-up Resistor Enable/Disable for P8-P15 | Read/Write | 0x00 |
| 0x0A | IER1 - Input Interrupt Enable for P0-P7 | Read/Write | 0x00 |
| 0x0B | IER2 - Input Interrupt Enable for P8-P15 | Read/Write | 0x00 |
| 0x0C | TSCR1 - Output Three-State Control for P0-P7 | Read/Write | 0x00 |
| 0x0D | TSCR2 - Output Three-State Control for P8-P15 | Read/Write | 0x00 |
| 0x0E | ISR1 - Input Interrupt Status for P0-P7 | Read | 0x00 |
| 0x0F | ISR2 - Input Interrupt Status for P8-P15 | Read | 0x00 |
| 0x10 | REIR1 - Input Rising Edge Interrupt Enable for P0-P7 | Read/Write | 0x00 |
| 0x11 | REIR2 - Input Rising Edge Interrupt Enable for P8-P15 | Read/Write | 0x00 |
| 0x12 | FEIR1 - Input Falling Edge Interrupt Enable for P0-P7 | Read/Write | 0x00 |
| 0x13 | FEIR2 - Input Falling Edge Interrupt Enable for P8-P15 | Read/Write | 0x00 |
| 0x14 | IFR1 - Input Filter Enable/Disable for P0-P7 | Read/Write | 0xFF |
| 0x15 | IFR2 - Input Filter Enable/Disable for P8-P15 | Read/Write | 0xFF |

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### 1.2 Interrupts

The table below summarizes the interrupt behavior of the different register settings for the XRA1403.

**TABLE 3: INTERRUPT GENERATION AND CLEARING**

| GCR BIT | IER BIT | REIR BIT | FEIR BIT | IFR BIT | INTERRUPT GENERATED BY: | INTERRUPT CLEARED BY: |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | No interrupts enabled (default) | N/A |
| 1 | 1 | 0 | 0 | 0 | A rising or falling edge on the input | Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR) |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 1 | 1 | 1 | 0 | 0 | A rising edge on the input | Reading the GSR register |
| | | | | 1 | A rising edge on the input and remains high for more than 1075ns | |
| 1 | 1 | 0 | 1 | 0 | A falling edge on the input | Reading the GSR register |
| | | | | 1 | A falling edge on the input and remains low for more than 1075ns | |
| 1 | 1 | 1 | 1 | 0 | A rising or falling edge on the input | Reading the GSR register |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 0 | x | x | x | x | No interrupts in output mode | N/A |

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## 2.0 REGISTER DESCRIPTION

### 2.1 GPIO State Register 1 (GSR1) - Read-Only

The status of P7 - P0 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.2 GPIO State Register 2 (GSR2) - Read-Only

The status of P15 - P8 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

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### 2.3 Output Control Register 1 (OCR1) - Read/Write

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.4 Output Control Register 2 (OCR2) - Read/Write

When P15 - P8 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.5 Input Polarity Inversion Register 1 (PIR1) - Read/Write

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.6 Input Polarity Inversion Register 2 (PIR2) - Read/Write

When P15 - P8 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.7 GPIO Configuration Register 1 (GCR1) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up and reset, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.8 GPIO Configuration Register 2 (GCR2) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up and reset, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.9 Input Internal Pull-up Enable/Disable Register 1 (PUR1) - Read/Write

This register enables/disables the internal pull-up resistors for an input. Writing a '1' to these bits will enable the internal pull-up resistors. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.10 Input Internal Pull-up Enable/Disable Register 2 (PUR2) - Read/Write

This register enables/disables the internal pull-up resistors for an input. Writing a '1' to these bits will enable the internal pull-up resistors. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.11 Input Interrupt Enable Register 1 (IER1) - Read/Write

This register enables/disables the interrupts for an input. After power-up and reset, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See Table 3 for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.12 Input Interrupt Enable Register 2 (IER2) - Read/Write

This register enables/disables the interrupts for an input. After power-up and reset, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See Table 3 for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.13 Output Three-State Control Register 1 (TSCR1) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.14 Output Three-State Control Register 2 (TSCR2) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.15 Input Interrupt Status Register 1 (ISR1) - Read-Only

This register reports the input pins that have generated an interrupt. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.16 Input Interrupt Status Register 2 (ISR2) - Read-Only

This register reports the input pins that have generated an interrupt. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

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### 2.17 Input Rising Edge Interrupt Enable Register 1 (REIR1) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.18 Input Rising Edge Interrupt Enable Register 2 (REIR2) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.19 Input Falling Edge Interrupt Enable Register 1 (FEIR1) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.20 Input Falling Edge Interrupt Enable Register 2 (FEIR2) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

### 2.21 Input Filter Enable Register 1 (IFR1) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.22 Input Filter Enable Register 2 (IFR2) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | 3.6 Volts |
| Supply current | 160 mA |
| Ground current | 200 mA |
| External current limit of each GPIO | 25 mA |
| Total current limit for GPIO[15:8] and GPIO[7:0] | 100 mA |
| Total current limit for GPIO[15:0] | 200 mA |
| Total supply current sourced by all GPIOs | 160 mA |
| Operating Temperature | -40° to +85°C |
| Storage Temperature | -65° to +150°C |
| Power Dissipation | 200 mW |

## TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

| | |
|---|---|
| Thermal Resistance (24-QFN) | theta-ja = 38°C/W, theta-jc = 26°C/W |
| Thermal Resistance (24-TSSOP) | theta-ja = 84°C/W, theta-jc = 16°C/W |

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# ELECTRICAL CHARACTERISTICS

## *DC ELECTRICAL CHARACTERISTICS*

**UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC IS 1.65V TO 3.6V**

| SYMBOL | PARAMETER | LIMITS 1.8V ± 10% MIN | LIMITS 1.8V ± 10% MAX | LIMITS 2.5V ± 10% MIN | LIMITS 2.5V ± 10% MAX | LIMITS 3.3V ± 10% MIN | LIMITS 3.3V ± 10% MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.2 | -0.3 | 0.5 | -0.3 | 0.8 | V | Note 1 |
| $V_{IH}$ | Input High Voltage | 1.4 | 5.5 | 1.8 | 5.5 | 2.0 | 5.5 | V | Note 1 |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | V<br>V<br>V | $I_{OL}$ = 6 mA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 1.5 mA<br>Note 2 & Note 4 |
| $V_{OL}$ | Output Low Voltage | | 0.5 | | 0.5 | | 0.5 | V | $I_{OL}$ = 8 mA<br>Note 3 |
| $V_{OH}$ | Output High Voltage | 1.4 | | 1.8 | | 2.0 | | V<br>V<br>V | $I_{OL}$ = -4 mA<br>$I_{OL}$ = -2 mA<br>$I_{OL}$ = -0.2 mA<br>Note 2 |
| $V_{OH}$ | Output High Voltage | 1.2 | | 1.8 | | 2.6 | | V<br>V<br>V | $I_{OH}$ = -8 mA<br>$I_{OH}$ = -8 mA<br>$I_{OH}$ = -8 mA<br>Note 3 |
| $I_{IL}$ | Input Low Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| $I_{IH}$ | Input High Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| $C_{IN}$ | Input Pin Capacitance | | 5 | | 5 | | 5 | pF | |
| $I_{CC}$ | Power Supply Current | | 0.5 | | 1.0 | | 2.0 | mA | Test 1 |
| $I_{CC}$ | Power Supply Current | | 0.6 | | 1.2 | | 2.4 | mA | Test 2 |
| $I_{CCS}$ | Standby Current | | 1 | | 2 | | 5 | uA | Test 3 |
| $R_{GPIO}$ | GPIO pull-up resistance | 60 | 140 | 60 | 140 | 60 | 140 | kΩ | 100kΩ ± 40% |
| $R_{RESET\#}$ | Reset# pull-up resistance | 35 | 85 | 35 | 85 | 35 | 85 | kΩ | 60kΩ ± 40% |

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***NOTES:***

1. *For SPI input signals (SI, SCL) & GPIOs, A0, A1 and A2 signals;*
2. *For SPI output signal SO;*
3. *For GPIOs;*
4. *For IRQ# signal;*

Test 1: SCL frequency is 10 MHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 2: SCL frequency is 10 MHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. SCL and SI are at GND. CS# is at VCC. All GPIOs are configured as inputs. Outputs are left floating or in tri-state mode.

### *AC ELECTRICAL CHARACTERISTICS - SPI-BUS TIMING SPECIFICATIONS*

*Unless otherwise noted: TA=-40° to +85°C, Vcc=1.65V - 3.6V*

| Symbol | Parameter | Limits 1.8V ± 10% | | Limits 2.5V ± 10% | | Limits 3.3V ± 10% | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{SCL}$ | Operating frequency | | 15 | | 26 | | 26 | MHz | |
| $T_{CSS}$ | CS# to SCL setup time | 20 | | 20 | | 20 | | ns | |
| $T_{CSH}$ | CS# to SCL hold time | 20 | | 20 | | 20 | | ns | |
| $T_{DO}$ | SCL fall to SO valid time | | 100 | | 100 | | 100 | ns | $C_L$ = 30 pF |
| $T_{DS}$ | SI to SCL setup time | 20 | | 20 | | 20 | | ns | |
| $T_{DH}$ | SI to SCL hold time | 20 | | 20 | | 20 | | ns | |
| $T_{CP}$ | SCL period | 66 | | 38 | | 38 | | ns | $T_{CH} + T_{CL}$ |
| $T_{CH}$ | SCL HIGH time | 30 | | 15 | | 15 | | ns | |
| $T_{CL}$ | SCL LOW time | 30 | | 15 | | 15 | | ns | |
| $T_{CSW}$ | CS# HIGH pulse width | 30 | | 30 | | 30 | | ns | |
| $T_{D13}$ | SPI input pin interrupt clear | | 200 | | 200 | | 200 | ns | |

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**FIGURE 5. SPI-BUS TIMING**

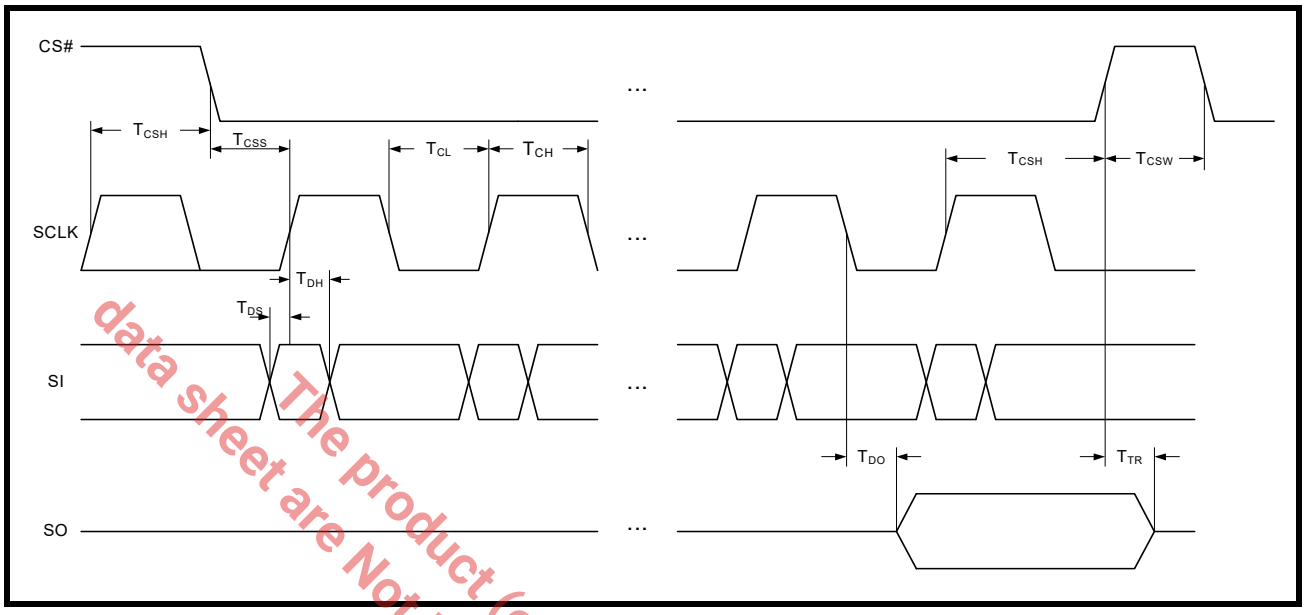
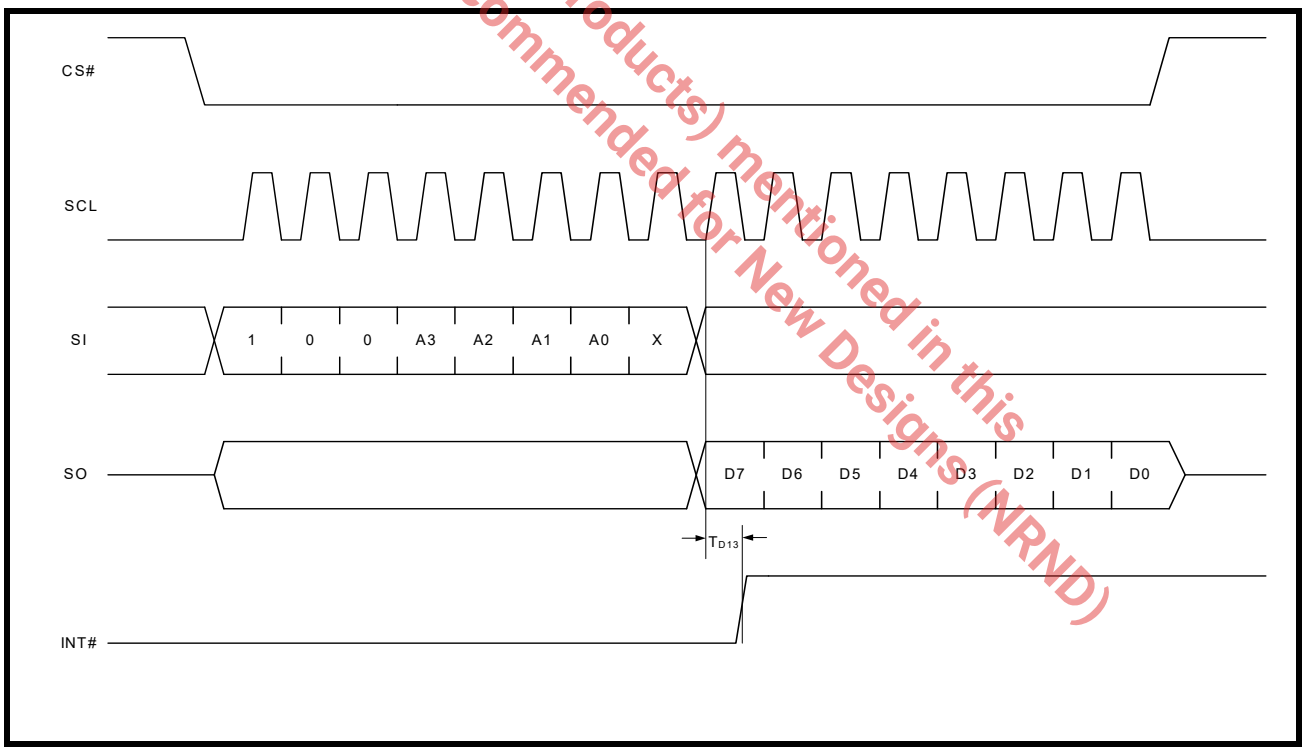
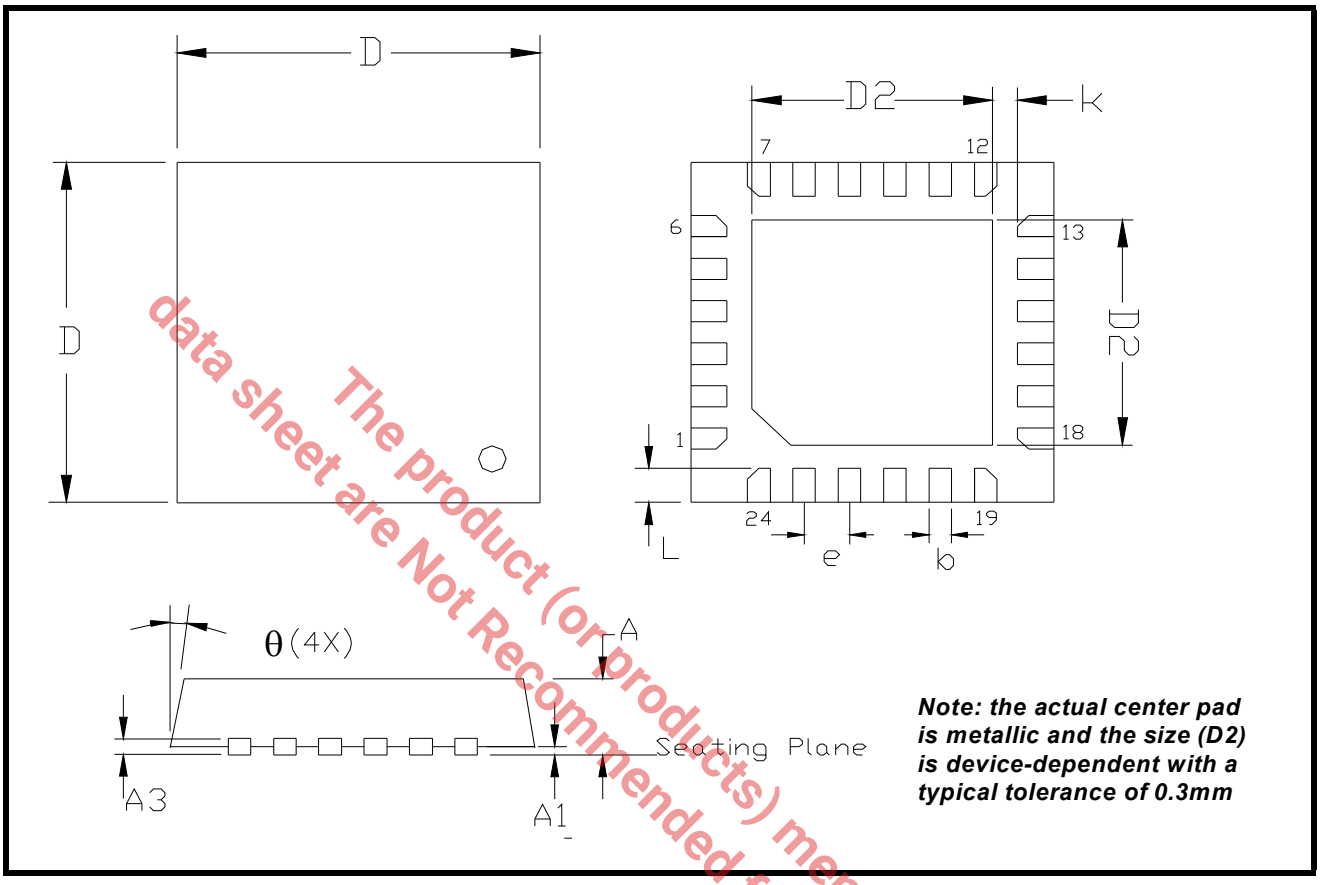



**FIGURE 6. READ INPUT PORT TO CLEAR GPIO INT**




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## PACKAGE DIMENSIONS (24 PIN QFN - 4 X 4 X 0.9 mm)



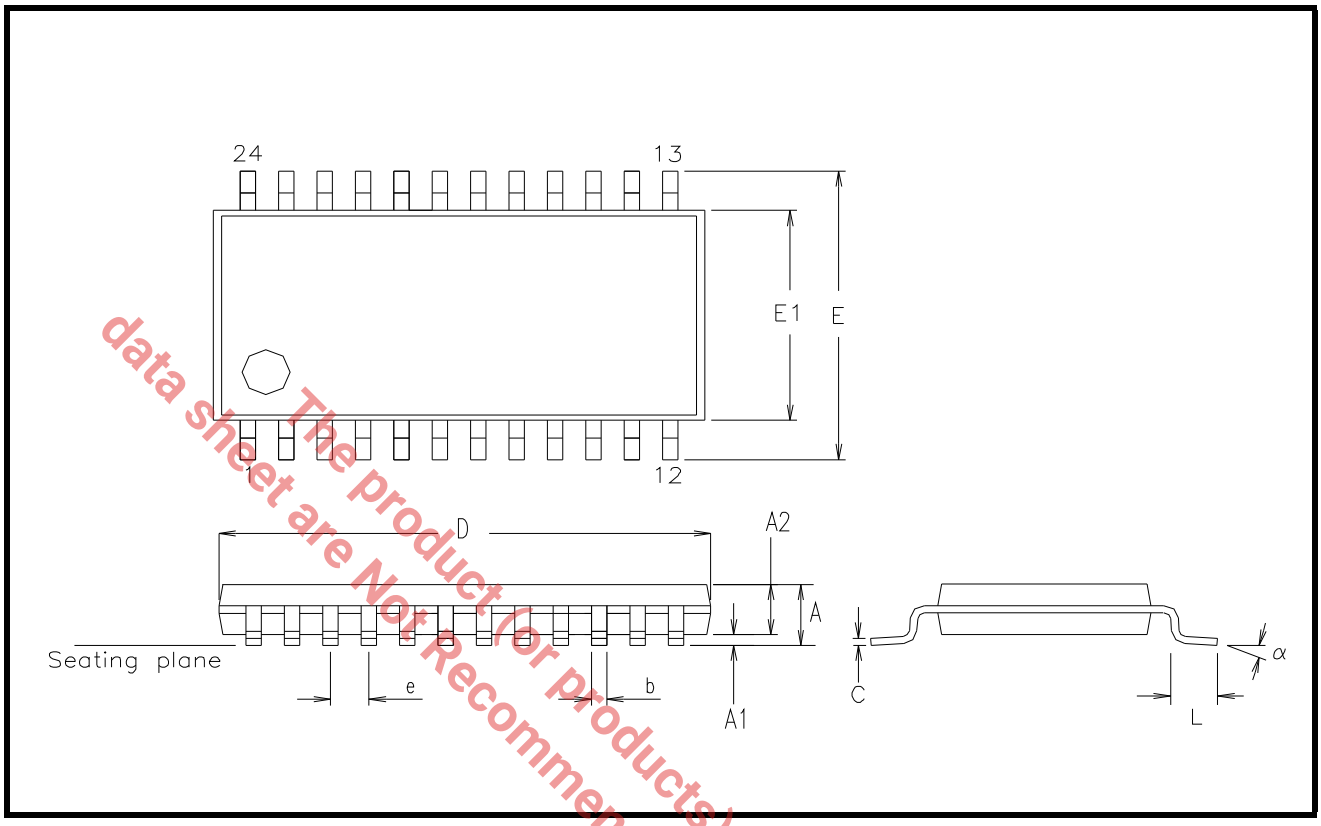

***Note: the actual center pad is metallic and the size (D2) is device-dependent with a typical tolerance of 0.3mm***

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

*Note: The control dimension is in millimeter.*

| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | - | 0.039 | - | 1.00 |
| A1 | 0.000 | 0.002 | 0.00 | 0.05 |
| A3 | 0.006 | 0.010 | 0.15 | 0.25 |
| θ | 0 | 14° | 0 | 14° |
| D | 0.154 | 0.161 | 3.90 | 4.10 |
| D2 | 0.087 | 0.102 | 2.20 | 2.60 |
| b | 0.007 | 0.012 | 0.18 | 0.30 |
| e | 0.020 BSC | | 0.50 BSC | |
| L | 0.012 | 0.020 | 0.30 | 0.50 |
| k | 0.008 | - | 0.20 | - |

## PACKAGE DIMENSIONS (24 PIN TSSOP - 4.4 mm)




data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

*Note: The control dimension is in millimeter.*

| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.031 | 0.047 | 0.80 | 1.20 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 |
| b | 0.007 | 0.012 | 0.19 | 0.30 |
| C | 0.004 | 0.008 | 0.09 | 0.2 |
| D | 0.303 | 0.311 | 7.70 | 7.90 |
| E | 0.240 | 0.264 | 6.10 | 6.70 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.0256 BSC | | 0.65 BSC | |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| α | 0° | 8° | 0° | 8° |

## REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| September 2011 | 1.0.0 | Final datasheet. |
| August 2020 | 1.0.1 | Update to MaxLinear logo. Update Ordering Information. |

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
760.692.0711 p.
760.444.8598 f.
www.maxlinear.com

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