XR46110

LED Current Controller with Line Regulation Compensation

Description

The XR46110 is an LED current controller with line regulation compensation for operating over a wide alternative current (AC) voltage source range. It can drive an external N-channel power MOSFET to regulate the current flowing through a high voltage (HV) LED string.

The application of the XR46110 is configured in series with an LED string, working as a constant current sink with linear type overvoltage protection (OVP), linear type over temperature protection (OTP), and line regulation compensation. It is suitable for applications with a rectified AC voltage source.

The PCB design can be very compact to meet various shape requirements. It is especially suitable for replacing incandescent light bulb and linear type fluorescent lamps.

FEATURES

- Device
  - 6V to 78V chip supply voltage range
  - Excellent system power regulation in ±10% AC mains fluctuation
  - Over temperature protection
  - Overvoltage protection
  - Single board LED lighting solution available
  - 2mm x 2mm TDFN-6 package
- System
  - All solid state components
  - No electrolytic capacitor required
  - Scalable architecture allows optimization of performance vs. cost
  - Driver-on-board and chip-on-board design solution available which minimize process flow and assembly cost
  - High PF and low THD performance
  - Flexible PCB layout options

APPLICATIONS

- LED Lighting Applications
  - Downlight
  - High bay
  - Specialty
  - Architectural

Typical Application

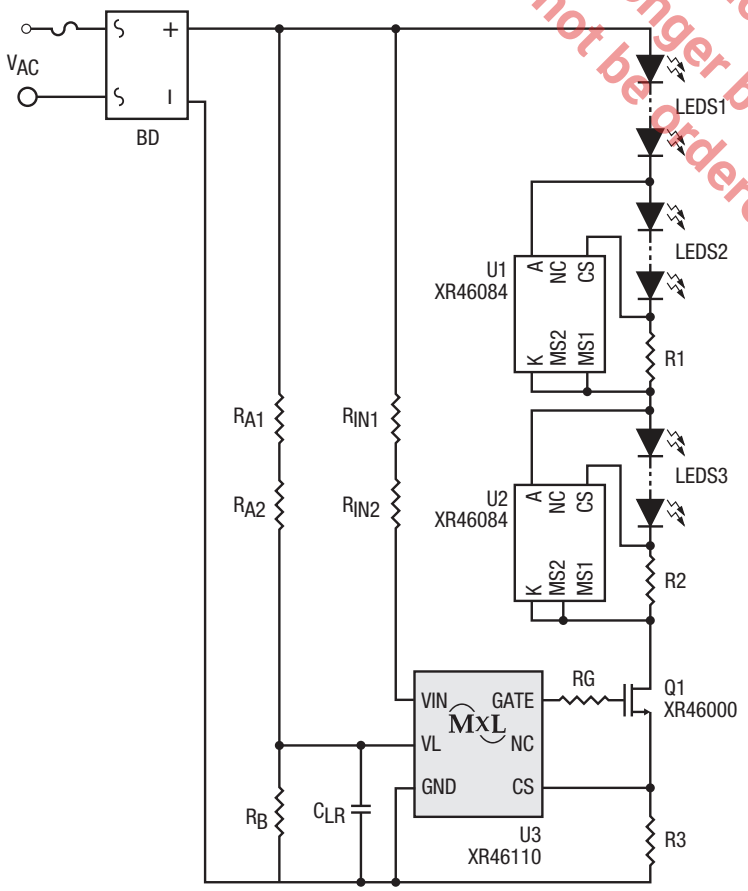


Figure 1. Typical Application

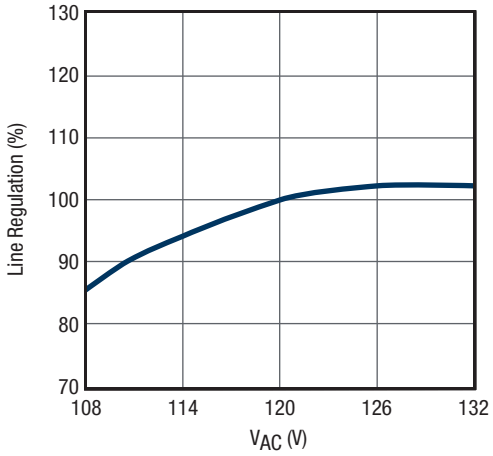


Figure 2. Line Regulation

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Sustaining voltage

- VIN, GATE to GND ..... -0.3V to 85V
- GATE to CS ..... -0.3V to 7V
- VL to GND..... -0.3V to 7V
- CS to GND ..... -0.3V to 1V

VIN input current..... 3mA

Maximum junction temperature, T_J..... 150°C

Storage temperature range ..... -55°C to 150°C

Lead temperature (soldering, 10 seconds)..... 260°C

ESD Rating (HBM - Human Body Model)..... 2kV

NOTES:

1. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.
2. All parameters having Min/Max specifications are guaranteed. Typical values are for reference purpose only.
3. Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$.

Operating Conditions

Input voltage

VIN.....6V to VIN_{Clamp}

Junction temperature range, T_J ..... -40°C to 125°C

Electrical Characteristics

Unless otherwise noted, typical values are at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN_{MIN}	Minimum VIN supply voltage		6			V
I_{IN}	VIN supply current	VIN = 6V to 73V		0.3		mA
VIN_{Clamp}	VIN overvoltage clamp	When VIN > VIN_{Clamp}, I_{IN} will increase to > 1mA to clamp VIN at VIN_{Clamp}	73	76	80	V
V_{CS}	CS voltage	VIN = 15V and 75V, V_{VL} = 1.75V	244	250	256	mV
ΔV_{LR1}	CS voltage line regulation vs. V_{VL}(1)	VIN = 15V and VIN = 75V, V_{VL} = 1.57V to 1.75V	-0.31	-0.28	-0.25	mV/mV
ΔV_{LR2}		VIN = 15V and VIN = 75V, V_{VL} = 1.75V to 2.10V	-0.27	-0.24	-0.21	
ΔV_{LR3}		VIN = 15V and VIN = 75V, V_{VL} = 2.10V to 2.28V	-0.33	-0.3	-0.27	
$V_{CS,Clamp}$	Maximum V_{CS} clamp	VL under voltage protection, V_{VL} < 1.45V	310	323	336	mV
V_{Gate}	Gate voltage	Gate to CS		5.4		V
I_{SOURCE}	GATE source current(2)	V_{Gate} - GND = 3V, V_{VL} = 1.75V, V_{CS} = 200mV		40		µA
I_{SINK}	GATE sink current(2)	V_{Gate} - GND = 3V, V_{VL} = 1.75V, V_{CS} = 500mV		4.2		mA
T_{TP}	Thermal protection trip temperature(2)	When T_J is higher than T_{TP}, V_{CS} decreases linearly	135	145		°C
$\Delta V_{CS}/\Delta TJ$	Thermal protection mode V_{CS} decreasing slope(2)	$T_J > T_{TP}$		-1.1		%/°C

NOTES:

1. The CS voltage line regulation is defined as:

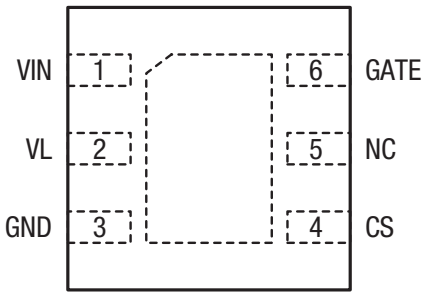
$$\Delta V_{LR1} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS(V_{VL}\,=\,1.75V)} - V_{CS(V_{VL}\,=\,1.57V)}}{1.75V - 1.57V}$$

$$\Delta V_{LR2} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS(V_{VL}\,=\,2.10V)} - V_{CS(V_{VL}\,=\,1.75V)}}{2.10V - 1.75V}$$

$$\Delta V_{LR3} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS(V_{VL}\,=\,2.28V)} - V_{CS(V_{VL}\,=\,2.10V)}}{2.28V - 2.10V}$$

2. Guarantee by design, not by production test.

Pin Configuration



2mm x 2mm TDFN-6, Top View

Pin Functions

Pin Number	Pin Name	Description
1	VIN	Power supply pin.
2	VL	Line regulation sense pin. The reference voltage is adjusted according to VL to provide the line regulation compensation and to provide overvoltage protection.
3	GND	Ground pin.
4	CS	Current sense pin. Connect a sense resistor, R_{CS}, between this pin adn the GND pin. The peak current is set by: $I_{OUT} = \frac{V_{CS}}{R_{CS}}$
5	NC	No connection.
6	GATE	External HV NMOS gate driving pin. Limited to 5.5V maximum.
Exposed Thermal Pad (EP)		Exposed thermal pad of the chip. Use this pad to enhance the power dissipation capability. The termal conductivity will be improved if a copper foil on PCB is soldered with the thermal pad. It is recommended to connect the exposed thermal pad to the GND pin.

Functional Block Diagram

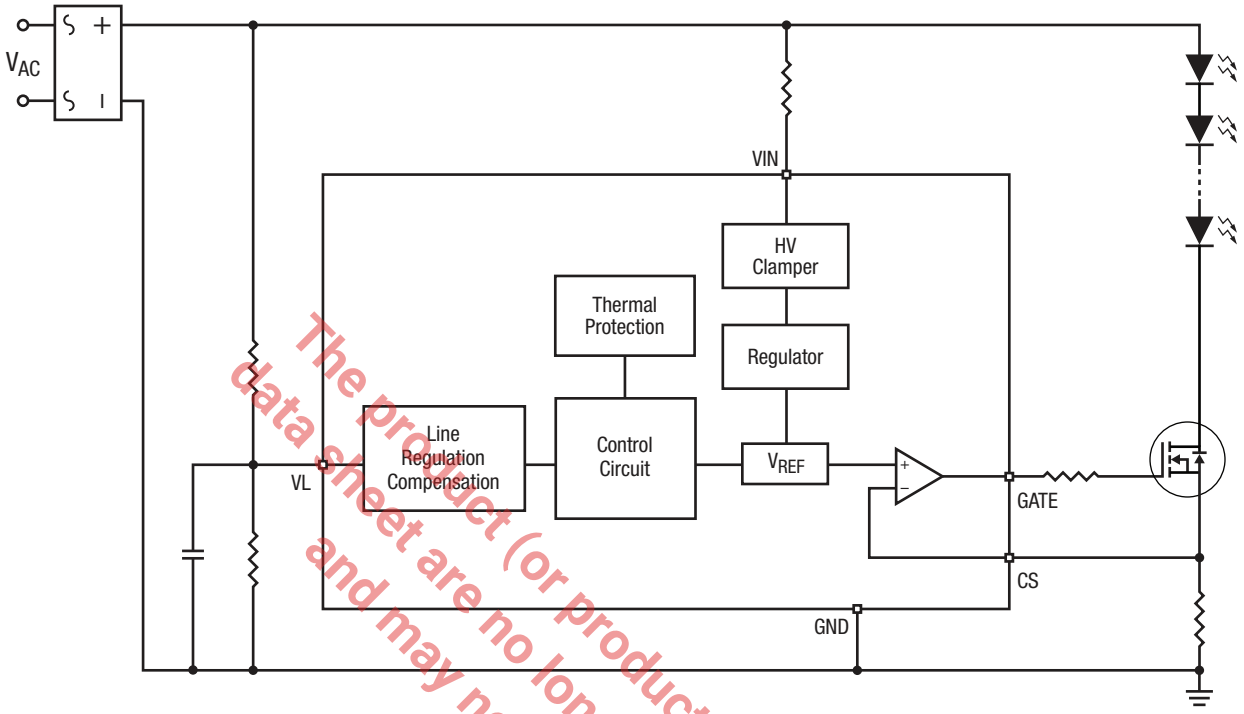


Figure 3. Functional Block Diagram

Applications Information

Typical Application Circuit

The XR46110 can work with XR46083 or XR46084 to support one or more steps fundamental driving structure, balance driving structure, low flicker driving structure, and phase cut dimmable driving structure. Two examples are shown in below.

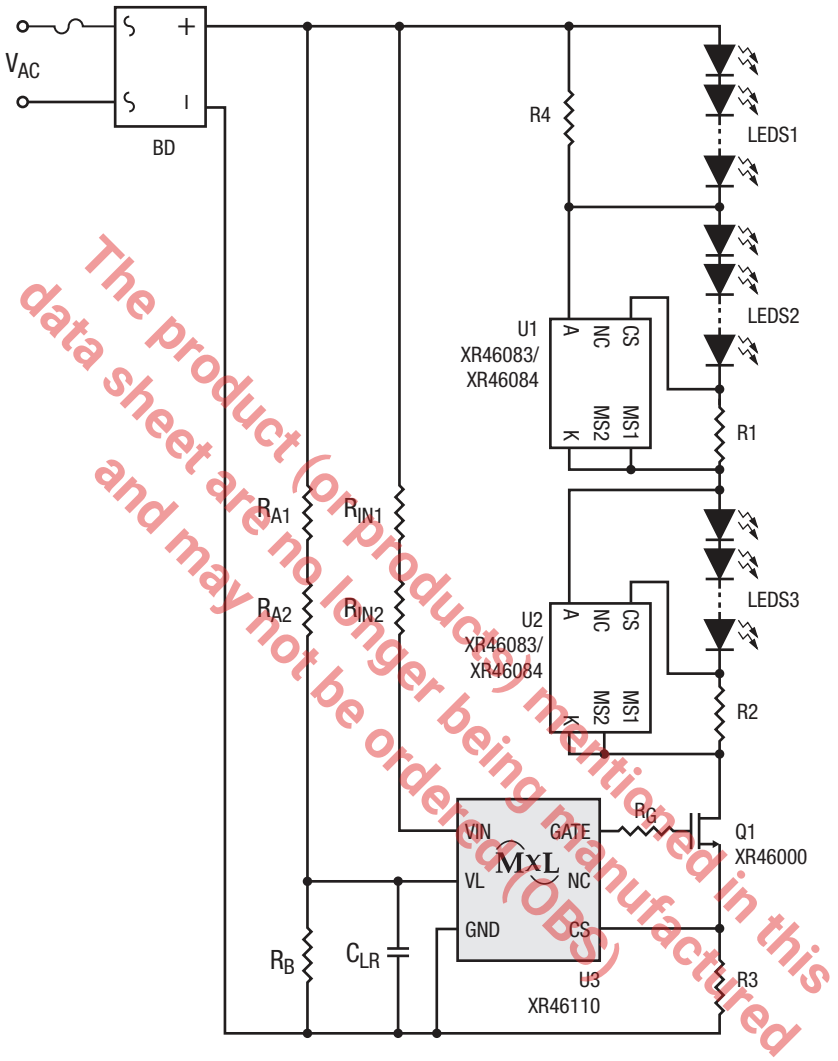


Figure 4. Fundamental 3-Step Structure

Applications Information (Continued)

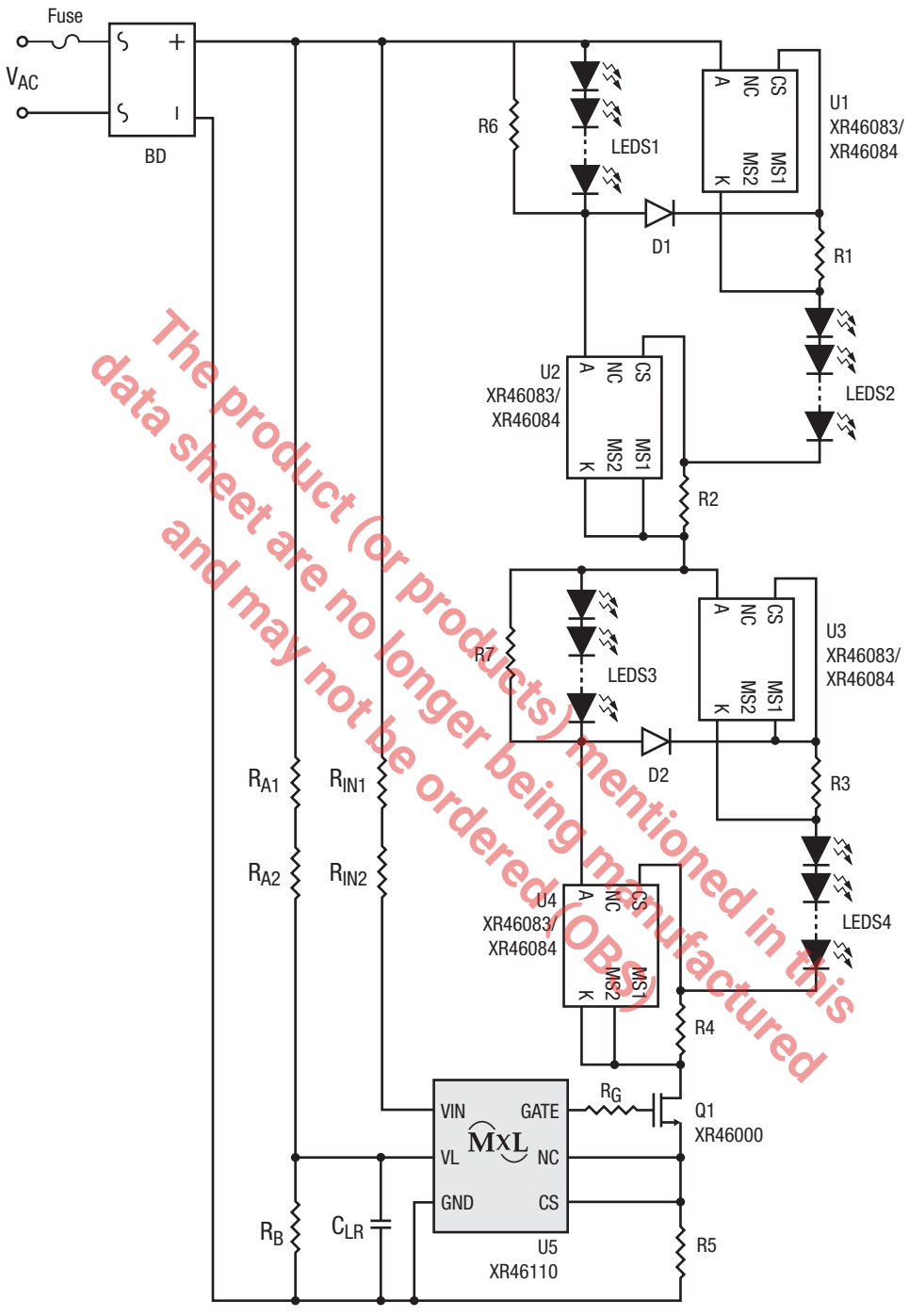


Figure 5. Balance 3-Step Structure

For a discussion regarding the basic circuit operation of MaxLinear's AC Step drivers, see XR46083 Application Notes.

Applications Information (Continued)

Linear Type Thermal Protection

When the junction temperature T_J rises to the Thermal Protection Trip Temperature T_{TP} (typically 145°C), the current sense voltage V_{CS} starts to decrease linearly at a slope of -1.1%/°C. The LED driving current decreases proportionally with the V_{CS} voltage. The system will function normally during the thermal protection mode with the lower driving current, but the power dissipation of the system will decrease until thermal equilibrium is reached.

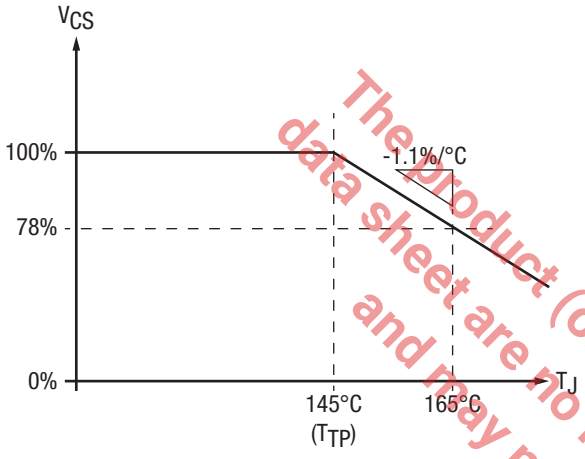


Figure 6. V_{CS} vs. T_J

Line Regulation Compensation

When there is variation in line voltage (V_{AC}), the power of the lamp will also change if the LED driving current is kept unchanged. In order to provide good line regulation when V_{AC} varies within a ±20% range, the average of the rectified V_{AC} is sensed by the VL pin to provide compensation in order to attempt to keep the power of the lamp at the same level.

The peak LED driving current is adjusted as the voltage level V_{VL} at the VL pin is changed. Based on the design, the LED driving current will be lower when V_{AC} is higher than the nominal value, and the LED driving current will be higher when V_{AC} is lower than the nominal value. The system power can then be maintained at approximately the same level. During power on, the driving current may be slightly higher for a few cycles until steady state is reached.

With the compensation function, the XR46110 provides excellent power line regulation over a ±20% VAC variation range, as shown in below.

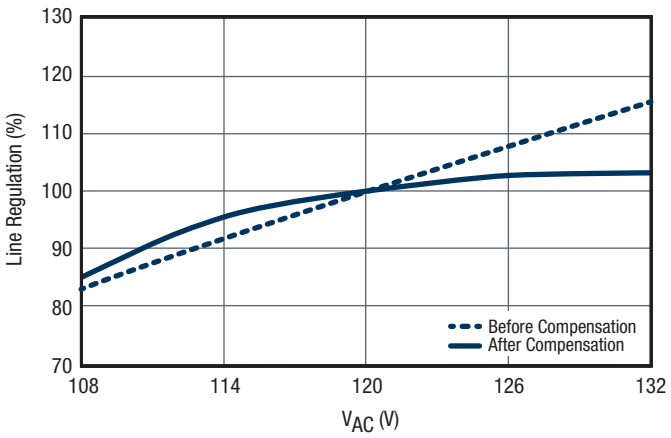


Figure 7. Power Line Regulation Compensation

Layout Suggestion

The exposed thermal pad under the chip is used to enhance the power dissipation capability. The thermal conductivity will be improved if a copper foil on PCB soldered with the thermal pad can be as large as possible. It is strongly recommended to connect the GND pin to the exposed thermal pad.

The external HV NMOS is recommended to be placed close to the chip. The current sense resistor connected between the CS pin and GND pin should be placed as close as to the CS pin and GND pin, as the example in below.

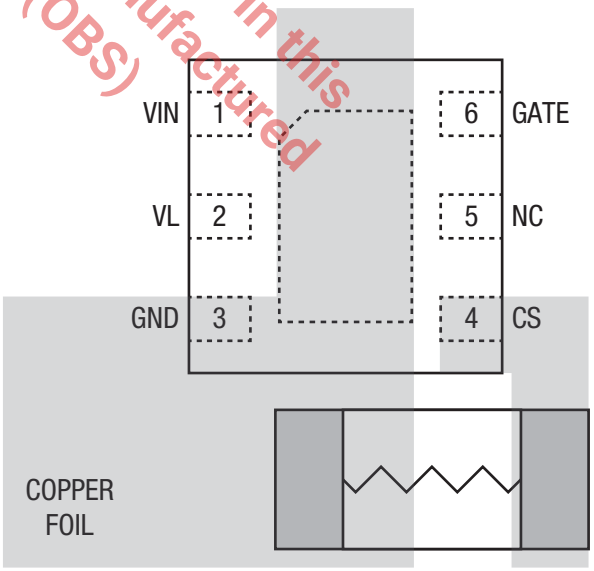
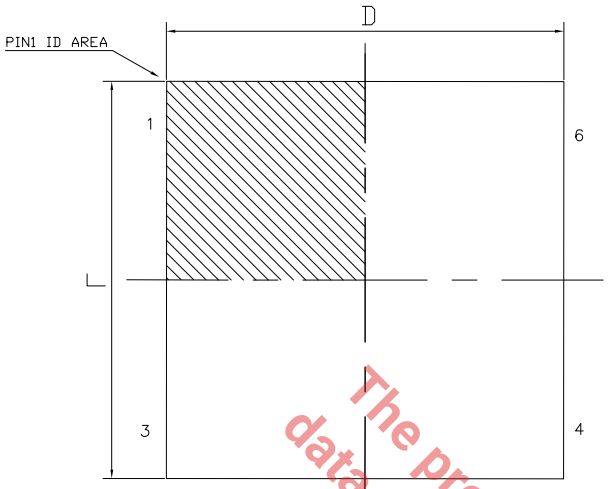
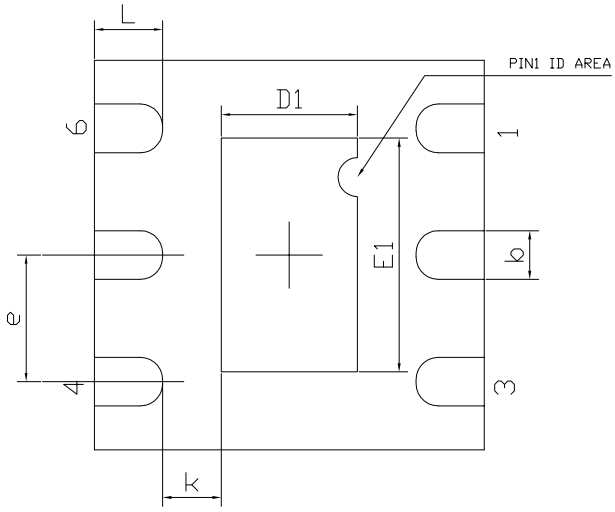


Figure 8. Layout

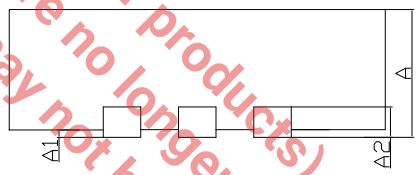
Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	–	0.050
A2	0.203Ref		
b	0.200	0.250	0.300
D	2.00 BSC		
E	2.00 BSC		
e	0.650 BSC		
D1	0.600	0.700	0.800
E1	1.100	1.200	1.300
L	0.274	0.350	0.426
K	0.200	–	–
N	6		

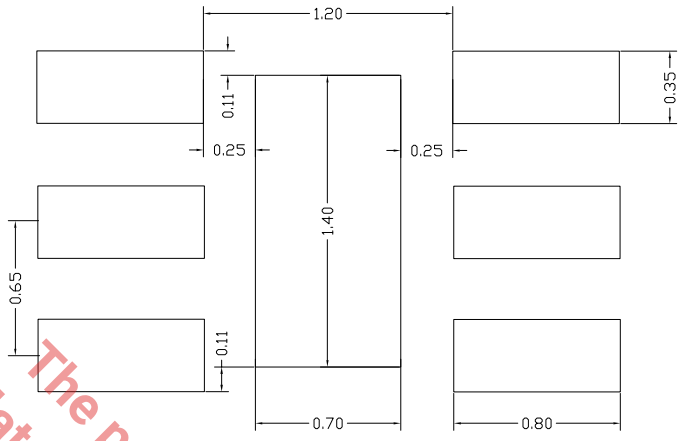
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-229.

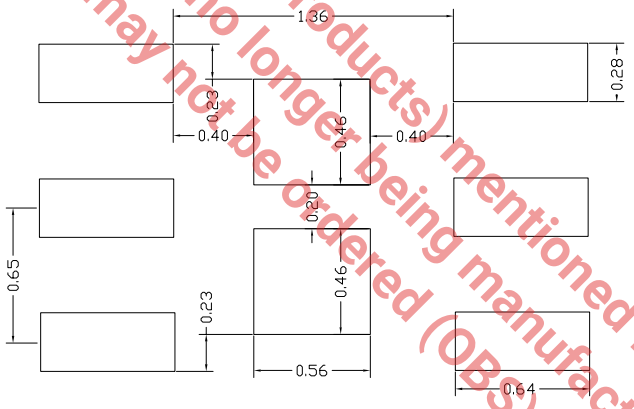
Drawing No.: POD-00000072

Revision: B

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000072

Revision: B

Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR46110IHBTR	-40°C ≤ T_J ≤ 125°C	Yes[2]	TDFN6 2x2	Tape and Reel

NOTE:
1. Refer to www.exar.com/XR46110 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1.0	Jul 2015	First release.
1A	Oct 2016	Change to new datasheet format and update Package Description.
1B	Mar 2017	Add ESD, clarified operating temperature, add CS voltage line regulation min/max, update GATE source and sink current test method.
1C	Aug 2018	Update to MaxLinear logo. Update format.

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

High Performance Analog:
1060 Rincon Circle
San Jose, CA 95131
Tel.: +1 (669) 265-6100
Fax: +1 (669) 265-6101
www.exar.com