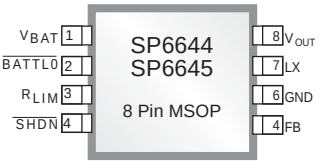
Single/Dual Alkaline Cell, High Efficiency Boost DC-DC Regulator

- 90mA Output Current at 1.3V Input
- 190mA Output Current at 2.6V Input
- +2V to +5.5V Output Range
- 0.88V Guaranteed Start-Up
- 92% High Efficiency
- 1.6µA Quiescent Supply Current at V_{BATT}
- Reverse Battery Protection
- Internal Synchronous Rectifier
- 5nA Logic Controlled Shutdown Current From V_{BATT}
- Low-Battery Detection Active LOW Output



Now Available in Lead Free Packaging

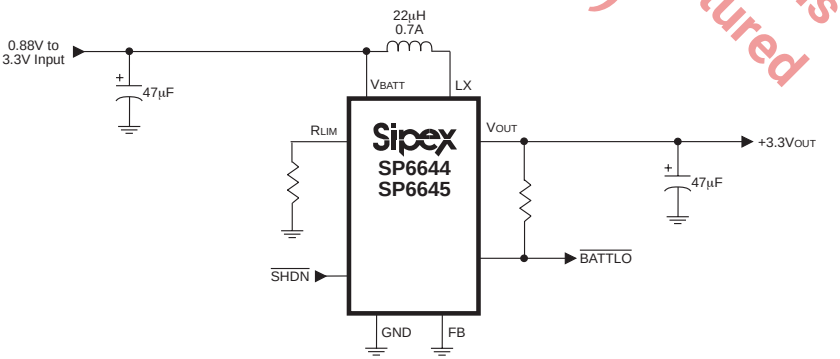
- Small 8 Pin MSOP Package
- No External FETs
- Flexibility to Optimize Inductor Type with Programmable Peak Current Control

The product(or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

DESCRIPTION

The SP6644/6645 devices are high-efficiency, low-power step-up DC-DC converters ideal for single or dual alkaline cell applications such as pagers, remote controls, pointing devices, medical monitors, and other low-power portable end products. Designers can control the SP6644 device with an active LOW shutdown input. The SP6644 device features an active low output for batteries below +1.0V. The SP6645 device features an active low output for batteries below +2.0V. Both devices contain a 0.8Ω synchronous rectifier, a 0.5Ω N-channel MOSFET power switch, an internal voltage reference, circuitry for pulse-frequency-modulation, and an under voltage comparator. The output voltage for the SP6644/6645 devices is preset to +3.3V ± 4% or can be adjusted from +2V to +5.5V by manipulating two external resistors

TYPICAL APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

V_{BATT} to GND.....-0.3 to 6.0V
V_{OUT} to GND.....-0.3 to 6.0V
LX, $\overline{SHDN}$, FB, $\overline{BATTLO}$, to GND.....-0.3 to 6.0V
Reverse battery Current, T_{AMB}=+25˚C.....220mA
(NOTE 1)
V_{BATT} forward current.....0.5A
V_{OUT}, LX current.....1A
Storage Temperature Range.....-65˚C to +165˚C
Lead Temperature (soldering 10s).....+300˚C
Operating Temperature.....-40˚C to +85˚C

Power Dissipation Per Package
8-pin µSOIC (derate 4.85mW/°C above +70°C).....390mW

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ELECTRICAL CHARACTERISTICS

V_{BATT} = $V_{\overline{SHDN}}$ = 1.3V, I_{LOAD} = 0mA, FB = GND, T_{AMB} = -40°C to +85°C, and typical values are at T_{AMB} = +25°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	♦	CONDITIONS
Maximum Operating Input Voltage, $V_{BATT(MAX)}$			3.3	V	♦	
Start-Up Input Voltage, V_{BATT}		0.82	1.1	V	♦	R_L = 3kΩ,
Start-Up Input Voltage, V_{BATT} Temperature Coefficient		-1		mV°C		
SHDN Input Voltage V_{IL} V_{IH}	 80		15	% 		% of V_{BATT} % of V_{BATT}
SHDN Input Current		1	100	nA	♦	
FB Input Current		1	100	nA	♦	V_{FB} =1.3V,
FB Set Voltage, V_{FB}	1.215	1.262	1.309	V	♦	external feedback
BATTLO Falling Trip Voltage	0.94 1.88	1.00 2.00	1.06 2.12	V	♦	SP6644, V_{OUT} = 3.3V SP6645, V_{OUT} = 3.3V
Output Voltage, V_{OUT}	3.16	3.30	3.44	V	♦	V_{FB}<0.1V
Output Voltage Range	2.0		5.5	V	♦	external feedback
N-Channel On-Resistance		0.5	1.0	Ω		V_{OUT} = 3.3V
P-Channel On-Resistance		0.8	1.6	Ω		V_{OUT} = 3.3V

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V_{BATT} = $V_{\overline{SHDN}}$ = 1.3V, I_{LOAD} = 0mA, FB = GND, T_{AMB} = -40°C to +85°C, and typical values are at T_{AMB} = +25°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
Quiescent Current into V_{OUT}, I_{QOUT}		50	80	µA	♦	V_{OUT} = 3.5V
Quiescent Current into V_{BATT}, I_{QBATT}		1.6	3.0	µA	♦	V_{BATT} = 1.0V
Shutdown Current into V_{OUT}, $I_{SHDNOUT}$		0.001	0.5	µA	♦	V_{OUT} = 3.5V, V_{SHDN} - 0V
Shutdown Current into V_{BATT}, $I_{SHDNBATT}$		0.005	0.1	µA	♦	V_{BATT} = 1.0V, V_{SHDN} - 0V
Low Output Voltage for $\overline{BATTLO}$, V_{OL}			0.4	V	♦	V_{BATT} = 0.9V,V_{OUT} = +3.3V,I_{SINK} =1mA
Leakage Current for $\overline{BATTLO}$			1	µA	♦	V_{BATT} = 2.6V,$V_{\overline{BATTLO}}$ = 3.5V
Efficiency		89		%	♦	I_{LOAD} = 150mA,V_{BATT} = 2.6V
Inductor Peak Current, I_{PEAK}	275	350	400	mA	♦	R_{LIM} = 5kΩ, NOTE 3
Under Voltage Lock-out (UVLO)	0.500	0.720		V	♦	

NOTE 1: The reverse battery current is measured from the Typical Operating Circuit's input terminal to GND when the battery is connected backward. A reverse current of 220mA will not exceed package dissipation limits but, if left for an extended time (more than 10 minutes), may degrade performance.
NOTE 2: Specifications to -40°C are guaranteed by design, not production tested.

NOTE 3: Inductor Peak Current where $I_{PEAK} = \frac{1400}{R_{LIM}}$

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

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PERFORMANCE CHARACTERISTICS

Refer to the circuit in *Figure 28*, T_{AMB} = +25°C unless otherwise noted.

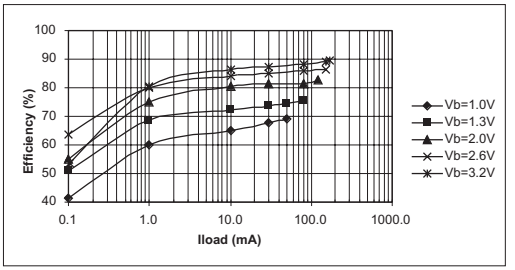


Figure 1. Efficiency vs. Output Current (Vout=3.3V), Rlim=2.5k, Li=22uH Sumida CD43

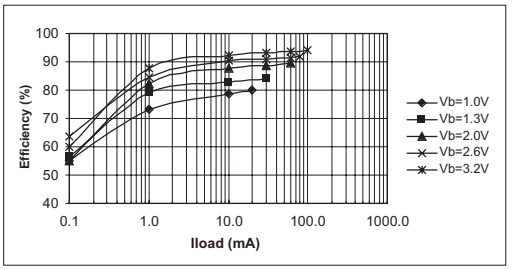


Figure 2. Efficiency vs. Output Current (V_{OUT}=3.3V), Rlim=5k, Li=22µH Sumida CD43

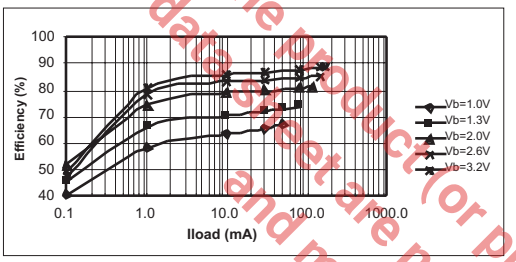


Figure 3. Efficiency vs. Output Current (Vout=3.3V), Rlim=2.5k, Li=22uH Sumida CDRH5D18 Low Profile

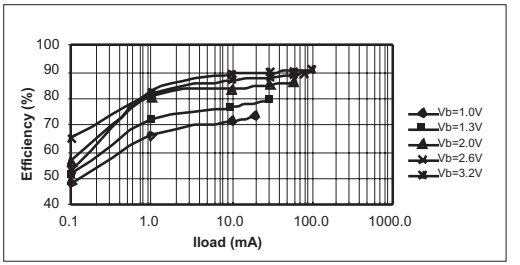


Figure 4. Efficiency vs. Output Current (Vout=3.3V), Rlim=5k, Li=100µH Sumida CD54

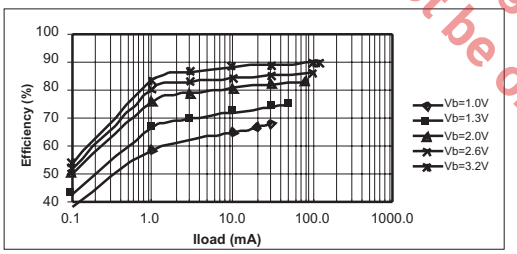


Figure 5. Efficiency vs. Output Current (Vout=5V), Rlim=2.5k, Li=22uH Sumida CD43, Refer to Figure 29, R1=499k, R2=169k

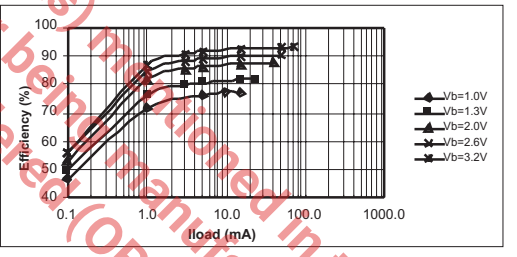


Figure 6. Efficiency vs. Output Current (Vout=5V), Rlim=5k, Li=22uH Sumida CD43, Refer to Figure 29, R1=499k, R2=169k

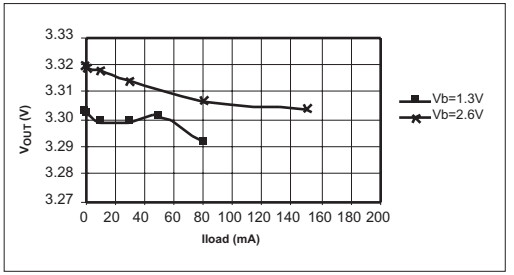


Figure 7. Line/Load Rejection vs. Output Current (Vout=3.3V), Rlim=2.5k, Li=22uH Sumida CD43

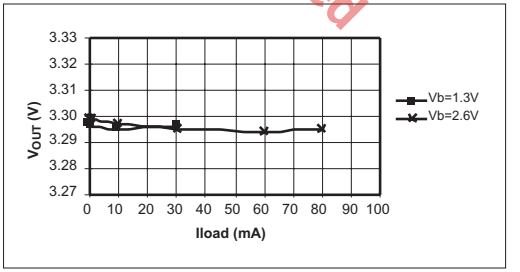


Figure 8. Line/Load Rejection vs. Output Current (Vout=3.3V), Rlim=5k, Li=22uH Sumida CD43

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Refer to the circuit in *Figure 28*, T_{AMB} = +25°C unless otherwise noted.

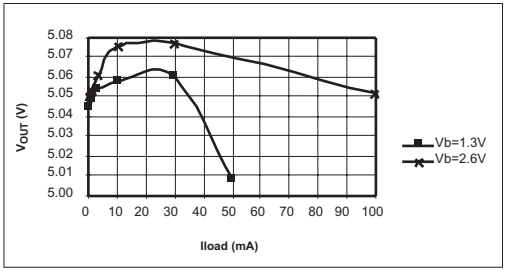


Figure 9. Line/Load vs. Output Current (Vout=5V), Rlim=2.5k, Li=22uH Sumida CD43, Refer to figure 29, R1=499k, R2=169k

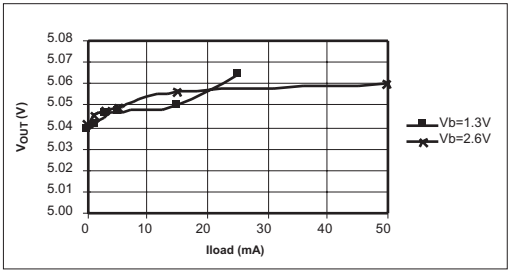


Figure 10. Line/Load vs. Output Current (Vout=5V), Rlim=5k, Li=22uH Sumida CD43, Refer to figure 29, R1=499k, R2=169k

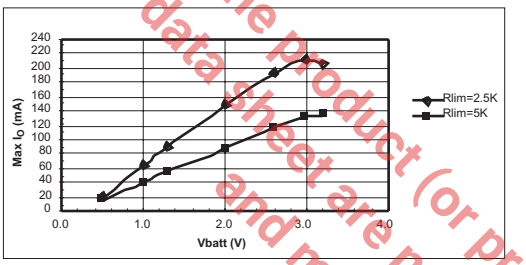


Figure 11. Maximum Load Current vs. Vbatt (Vout=3.3V), Li=22uH Sumida CD43

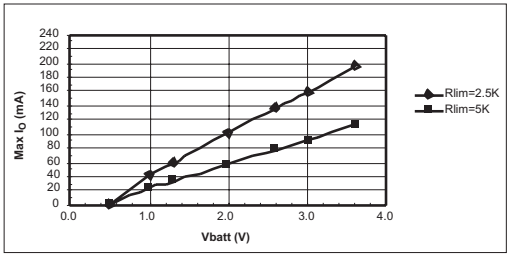


Figure 12. Maximum Load Current vs. Vbatt (Vout=5V), Li=22uH Sumida CD43, Refer to Figure 29, R1=499k, R2=169k

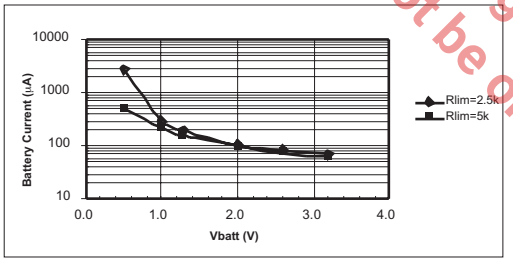


Figure 13. No Load Battery Current vs. Vbatt (Vout=3.3V), Li=22uH Sumida CD43

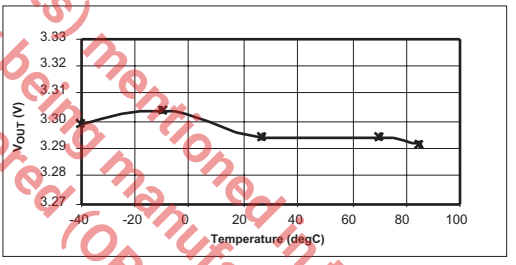


Figure 14. Output Voltage vs. Temperature, Rlim=2.5k, Rload=3k, (Vout=3.3V),Li=22uH Sumida CD43

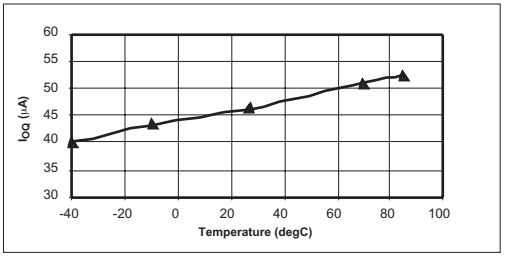


Figure 15. Io Pin Quiescent Current vs. Temperature, (Vout=3.3V)

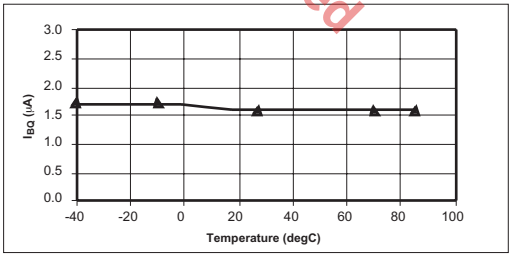


Figure 16. Ibatt Pin Quiescent Current vs. Temperature, (Vout=3.3V), Vbatt=1.0V

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Refer to the circuit in *Figure 28*, T_{AMB} = +25°C unless otherwise noted.

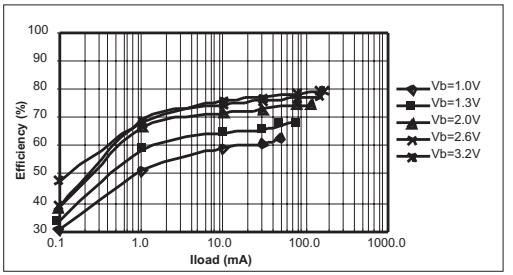


Figure 17. SP6644/6201 DC/DC LDO Combination Efficiency vs. Output Current (Vout=3.3V), Rlim=2.5k, Li=22µH Sumida CD-43, Refer to Figure 30

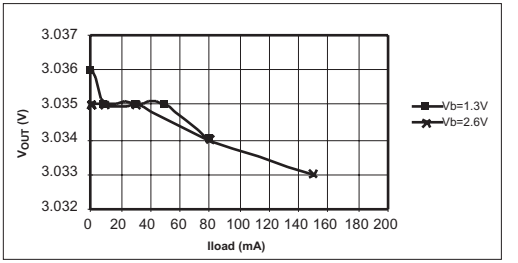


Figure 18. SP6644/6201 LDO Line/Load Rejection vs. Output Current (Vout=3.3V), Rlim=2.5k, Li=22µH Sumida CD-43, Refer to Figure 30

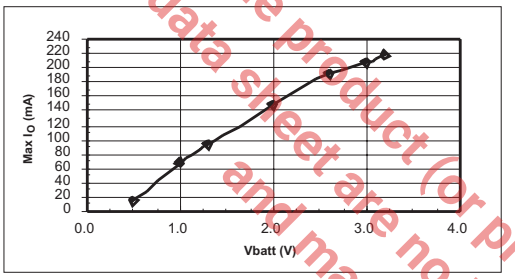


Figure 19. SP6644/6201 DC/DC LDO Maximum Load Current vs. Vbatt (Vout=3.3V), Rlim=2.5k, Li=22µH Sumida CD-43, Refer to Figure 30

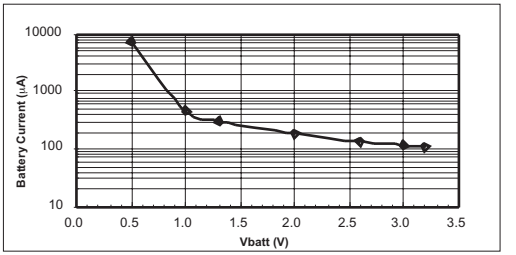


Figure 20. SP6644/6201 DC/DC LDO No-Load Ibatt vs. Vbatt (Vout=3.3V), Rlim=2.5k, Li=22µH Sumida CD-43, Refer to Figure 30

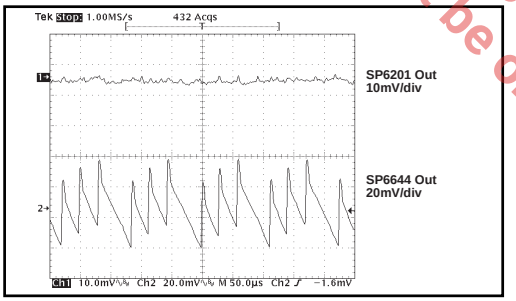


Figure 21. SP6644/6201 DC/DC LDO Output Ripple Voltage (Vout=3.3V), Rlim=2.5k, Li=22µH Sumida CD-43, Refer to Figure 30

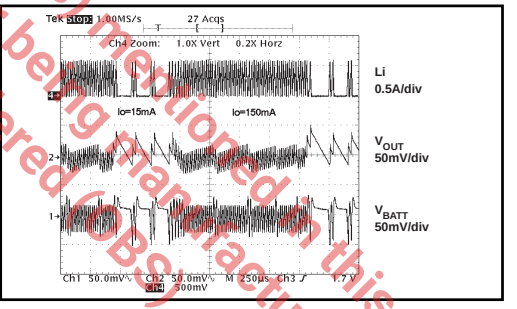


Figure 22. Load Transient Response, Vbatt=1.3V, (Vout=3.3V), Rlim=2.5k, Li=22µH Sumida CD-43

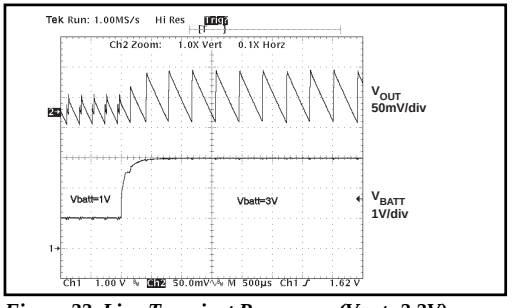


Figure 23. Line Transient Response, (Vout=3.3V), Rlim=2.5k, Iload=22µH Sumida CD-43

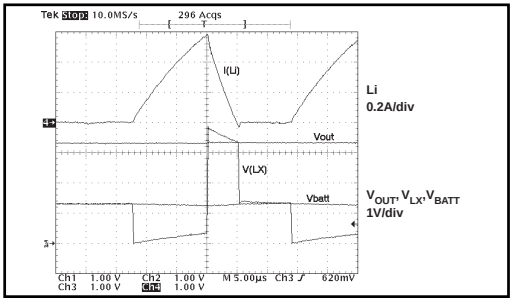


Figure 24. Switching Waveforms, (Vout=3.3V), Vbatt=1.3V, Rlim=2.5k, Iload=10mA, Li=22µH Sumida CD-43

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

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PERFORMANCE CHARACTERISTICS

Refer to the circuit in *Figure 28*, T_{AMB} = +25°C, unless otherwise noted.

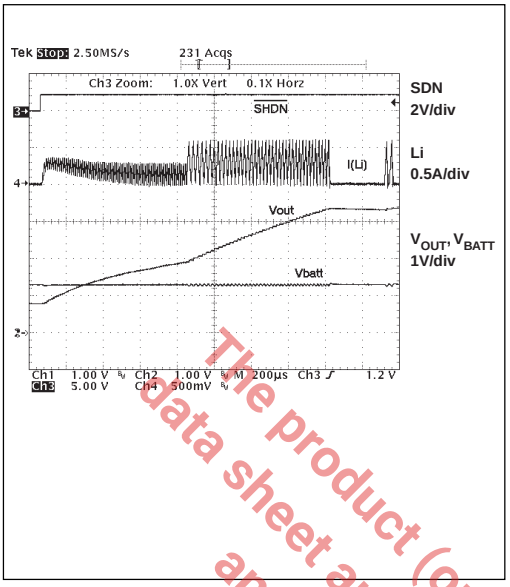


Figure 25. Shutdown Response and Inductor Current, Vout=3.3V, Vbatt=1.3V, Rlim=2.5k, Rload=550 Ohms, Li=22uH Sumida CD43

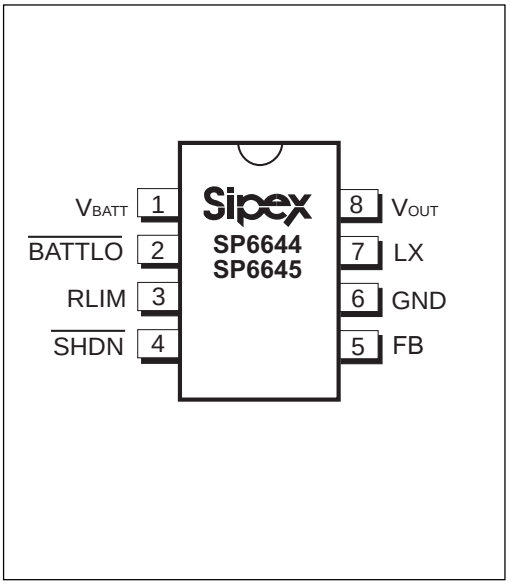


Figure 26. Pinout for the SP6644/6645

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (Obs).

PIN DESCRIPTION

NAME	FUNCTION	PIN NO.
V_{BATT}	Battery Supply. This pin ties to the sensor input of the $\overline{BATTLO}$ comparator.	1
$\overline{BATTLO}$	Open-Drain Battery Low Output. When the voltage drops below 1V for the **SP6644** or 2V for the **SP6645**, $\overline{BATTLO}$ sinks current.	2
R_{LIM}	Resistor Programmable Inductor Peak Current. Connecting a resistor from this pin to ground programs the inductor peak current where $I_{PEAK} = \frac{1400}{R_{LIM}}$	3
$\overline{SHDN}$	Active-LOW Shutdown Input. Connect to V_{BATT} for normal operation.	4
FB	Feedback Input. Input for adjustable-output operation. Connect this input pin to an external resistor voltage divider between V_{OUT} and GND. Connect to GND for fixed-output operation.	5
GND	Connect to the lowest circuit potential, typically ground.	6
LX	Coil. An inductor is connected from V_{BATT} to the N-Channel MOSFET switch drain and the P-Channel synchronous-rectifier drain through this pin.	7
V_{OUT}	Power Output. Feedback input for fixed 3.3V operation and IC power input. Connect filter capacitor close to V_{OUT}.	8

Table 1. SP6644/6645 Pin Descriptions

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DESCRIPTION

The SP6644/6645 devices are high-efficiency, low-power step-up DC-DC converters ideal for single or dual alkaline cell applications such as pagers, remote controls, and other low-power portable end products.

The SP6644/6645 devices feature a 5nA logic-controlled shutdown mode and a dedicated low-battery detector circuitry. Both devices contain a 0.8Ω synchronous rectifier, a 0.5Ω N-channel MOSFET power switch, an internal voltage reference, circuitry for pulse-frequency-modulation, and an under voltage comparator. The output voltage for the SP6644/6645 devices can be adjusted from +2V to +5.5V by manipulating two external resistors. The output voltage is preset to +3.3V.

THEORY OF OPERATION

The SP6644/6645 devices are ideal for end products that function with a single or dual alkaline cell, such as remote controls, pagers, and other portable consumer products. Designers can implement the SP6644/6645 devices into applications with the following power management operating states: 1. where the primary battery is good and the load is active, and 2. where the primary battery is good and the load is sleeping.

In the first operating state where the primary supply is good and the load is active, the SP6644/6645 devices typically offer 88% efficiency, drawing tens of milliamps.

Applications will predominantly operate in the second state where the primary supply is good and the load is sleeping. The SP6644/6645 devices draw a very low quiescent current while the load in its disabled state will draw typically hundreds of microamps.

The pulse-frequency-modulation (PFM) circuitry provides higher efficiencies at low to moderate output loads than traditional PWM converters are capable of delivering.

In a state where the error comparator detects that the output voltage at V_{OUT} is too low, the internal N-channel MOSFET switch is turned on until the peak inductor current is satisfied. This is indicated by the falling edge of the I-Charge comparator output. The approximate inductor charging time is defined by:

$$t_{CHARGE} \cong L \times I_{PEAK} / V_{BATT}$$

where t_{CHARGE} [s] is the approximate inductor charging time, L [H] is the inductance, I_{PEAK} [A] is the peak inductor current, and V_{BATT} [V] is the input voltage to the device.

The peak inductor current, I_{PEAK}, is programmed externally by putting a resistor between the R_{LIM} pin and ground. This is defined by:

$$I_{PEAK} = \frac{1400}{R_{LIM}}$$

where I_{PEAK} [A] is the peak inductor current and R_{LIM} [Ω] is the value of the resistor connected from pin R_{LIM} to ground.

When the charging N MOSFET turns off, the discharging P MOSFET turns on and the inductor current flows into the output capacitor and the load recharging the output. When the current through the discharging P MOSFET approaches zero, the I-Discharge comparator indicates to the logic to turn off the P MOSFET. The approximate time for discharging the inductor current can be determined by:

$$t_{DCHG} \cong \frac{L \times I_{PEAK}}{V_{OUT} - V_{BATT}}$$

where t_{DCHG} [s] is the time to discharge the inductor, L [H] is the inductance, I_{PEAK} [A] is the peak inductor current, V_{OUT} [V] is the output voltage, and V_{BATT} [V] is the input voltage to the device.

The output filter capacitor stores charge while current from the inductor is high and holds the output voltage high until the discharge phase of the next switching cycle, smoothing power flow to the load. Between switching cycles, the inductor damping switch is closed suppressing the ringing caused by the inductor and the parasitic capacitance on the LX node.

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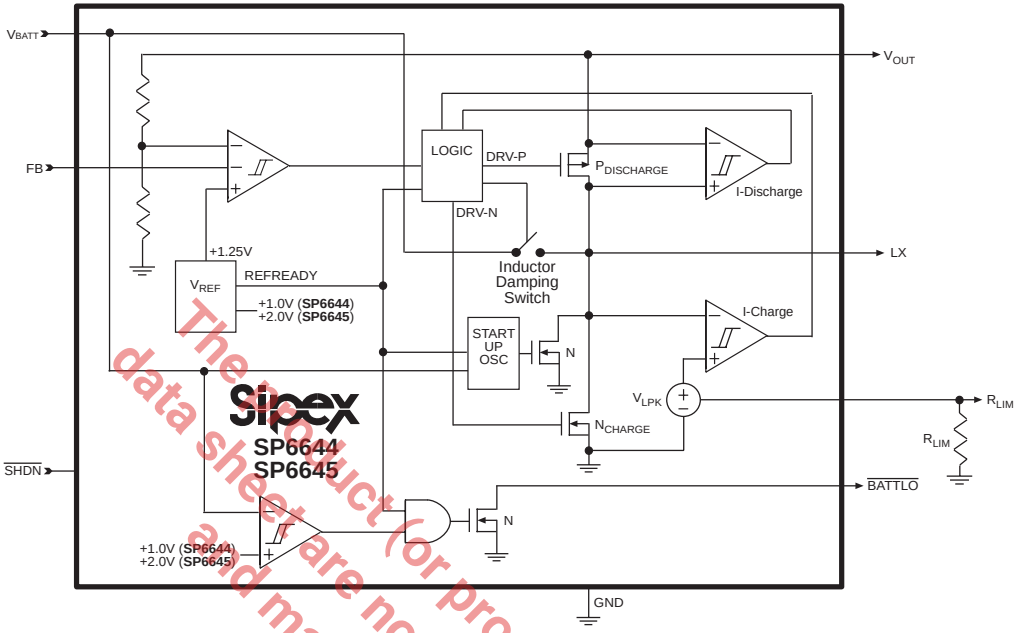


Figure 27. Internal Block Diagram of the SP6644/6645

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Internal Bootstrap Circuitry

The internal bootstrap circuitry contains a low-voltage start-up oscillator that pumps up the output voltage to approximately 1.9V so the main DC-DC converter can function. At lower battery supply voltages, the circuitry can start up with low-load conditions. Designers can reduce the load as needed to allow start-up with input voltages below 1V. Refer to *Figures 10* to *13*. Once started, the output voltage can maintain the load as the battery voltage decreases below the initial start-up voltage. The start-up oscillator is powered by V_{BATT} driving a charge pump and NMOS switch. During start-up, the P-channel synchronous rectifier remains off and either its body diode or an external diode is used as an output rectifier.

BATTLO Circuitry

The SP6644 device has an internal comparator for low-battery detection. If V_{BATT} drops below 1V, $\overline{BATTLO}$ will sink current. $\overline{BATTLO}$ is an open-drain output. The SP6645 operates in the same manner with a threshold voltage of 2V.

Shutdown for the SP6644

A logic LOW at $\overline{SHDN}$ will drive the SP6644 into a shutdown mode where $\overline{BATTLO}$ goes into a high-impedance state, the internal switching MOSFET turns off, and the synchronous rectifier turns off to prevent reverse current from flowing from the output back to the input. Designers should note that in shutdown, the output can drift to one diode drop below V_{BATT} because there is still a forward current path through the synchronous-rectifier body diode from the input to the output. To disable the shutdown feature, designers can connect $\overline{SHDN}$ to V_{BATT}.

Adjustable Output Voltage

Driving FB to ground (logic LOW) will drive the output voltage to the fixed-voltage operation of +3.3V ± 4%. Connecting FB to a voltage divider between V_{OUT} and ground will select an adjustable output voltage between +2V and +5.5V. Refer to *Figure 28*. FB regulates to +1.25V.

Since the FB leakage current is 10nA maximum, designers should select the feedback resistor R2 in the 100kΩ to 1MΩ range. R1 can be determined with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{V_{REF}} - 1 \right]$$

where R1 [Ω] and R2 [Ω] are the feedback resistors in *Figure 29*, V_{OUT} [V] is the output voltage, and V_{REF} [V] is 1.25V.

Battery Reversal Protection

The SP6644/6645 devices will tolerate single-cell battery reversal up to the package power-dissipation limits noted in the **ABSOLUTE MAXIMUM RATINGS** section. An internal diode in series with an internal 5Ω resistor limits any reverse current to less than 220mA preventing damage to the devices. Prolonged operation above 220mA reverse-battery current can degrade performance of the devices.

The Inductor

The programmable peak inductor current feature of the SP6644/6645 devices affords a great deal of flexibility in choosing an inductor. The most important point to consider when choosing an inductor is to insure that the peak inductor current is programmed below the saturation rating of the inductor. If the inductor goes into saturation, the internal switches and the inductor will be stressed due to current peaking, potentially leading to reliability problems with the application circuit.

The peak inductor current is programmed by putting a resistor between the R_{LIM} pin and ground. The usable current range is between 150mA and 560mA. This is defined by:

$$I_{PEAK} = \frac{1400}{R_{LIM}}$$

where I_{PEAK} [A] is the peak inductor current, and R_{LIM} [Ω] is the value of the resistor connected from pin R_{LIM} to ground.

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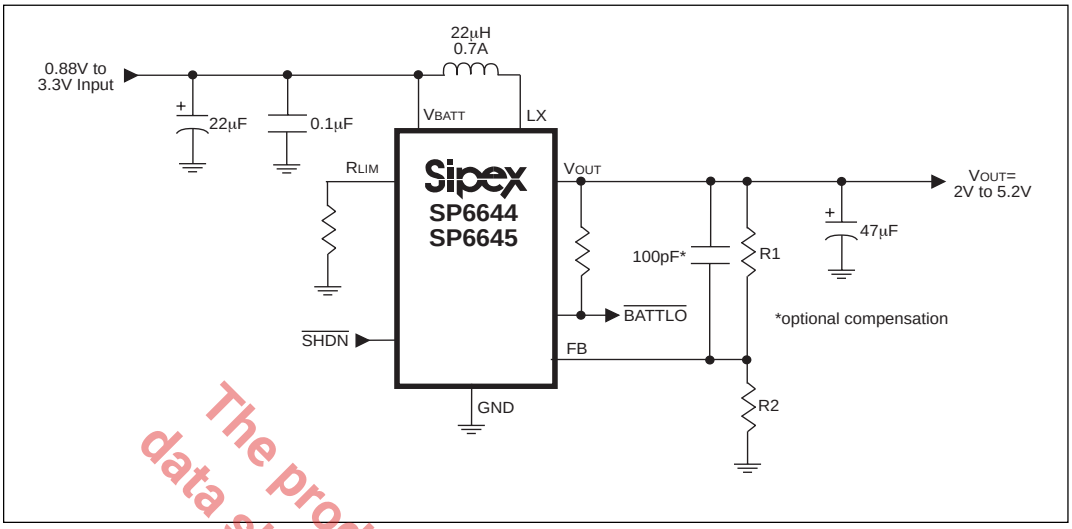


Figure 28. Adjustable Output Voltage Circuitry

With an external resistor tolerance of ±1%, the peak current tolerance will be ±6%. To make sure that the SP6644/6645 internal circuitry adequately controls the inductor current, it is recommended that values equal to or greater than 22µH (±10%) be used.

The SP6644/6645 devices control algorithm delivers an average maximum load current in regulation as defined by:

$$I_{LOAD\text{-}MAX} = \frac{E \times I_{PEAK} \times V_{BATT}}{2 \times V_{OUT}}$$

where $I_{LOAD\text{-}MAX}$ [A] is the maximum load current, E is the efficiency factor (generally between 0.8 and 0.9), I_{PEAK} [A] is the programmed peak inductor current, V_{BATT} [V] is the input voltage to the device, and V_{OUT} [V] is the output voltage.

Given the minimum input voltage, output voltage, and maximum average load current, the value of I_{PEAK} can be solved for and an appropriate inductor can be chosen. It is good design practice to use the lowest peak current possible to reduce possible EMI and output ripple voltage. A closed-core inductor, such as a toroid or shielded bobbin, will minimize any fringe magnetic fields or EMI.

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APPLICATION NOTES

Printed circuit board layout is a critical part of design. Poor designs can result in excessive EMI on the voltage gradients and feedback paths on the ground planes with applications involving high switching frequencies and large peak currents. Excessive EMI can result in instability or regulation errors.

All power components should be placed on the PC board as closely as possible with the traces kept short, direct, and wide (≥50mils or 1.25mm). Extra copper on the PC board should be integrated into ground as a pseudo-ground plane. On a multilayer PC board, route the star ground using component-side copper fill, then connect it to the internal ground plane using vias.

For the SP6644/6645 devices, the inductor and input and output filter capacitors should be soldered with their ground pins as close together as possible in a star-ground configuration. The V_{OUT} pin must be bypassed directly to ground as close to the SP6644/6645 devices as possible (within 0.2in or 5mm). The DC-DC converter and any digital circuitry should be placed on the opposite corner of the PC board as far away from sensitive RF and analog input stages. The external voltage-feedback network should be placed very close to the FB pin as well as the R_{LIM} resistor (within 0.2in or 5mm). Any

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noisy traces, such as from the LX pin, should be kept away from the voltage-feedback network and separated from it using grounded copper to minimize EMI.

Capacitor equivalent series resistance is a major contributor to output ripple, usually greater than 60%. Low ESR capacitors are recommended. Ceramic capacitors have the lowest ESR. Low-ESR tantalum capacitors may be a more acceptable solution having both a low ESR and lower cost than ceramic capacitors. Designers should select input and output capacitors with a rating exceeding the peak inductor current. Do not allow tantalum capacitors to exceed their ripple-current ratings. A 22µF, 6V, low-ESR, surface-mount tantalum output filter capacitor typically provides 60mV output ripple when stepping up from 1.3V to 3.3V at 20mA. An input filter capacitor can reduce peak currents drawn from the battery and improve efficiency. Low-ESR aluminum electrolytic capacitors are acceptable in some applications but standard aluminum electrolytic capacitors are not recommended.

Designers should add LC pi filters, linear post-regulators, or shielding in applications necessary to address excessive noise, voltage ripple, or EMI concerns. The LC pi filter's cutoff frequency should be at least a decade or two below the DC-DC converters's switching frequency for the specified load and input voltage.

A small SOT23-5pin 200mA Low Drop Out linear regulator can be used at the SP6644/6645 output to reduce output noise and ripple. The schematic in figure 29 illustrates this circuit with the SP6644 3.3V output followed by the Sipex SP6201 3.0V output Low Drop Out linear regulator. Compare in Figure 21 the SP6644 ripple of 40-50mVpp with the SP6201 ripple of about 3mVpp and you can see the amount of noise reduction obtained. Additional performance characteristics for the SP6644/6201 combination can be seen in figures 17 to 20.

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Inductance (uH)	Manufacturer/Part No.	Inductor Specification	
		Resistance (ohms)	Isat (mA)
22	Sumida CD43-220 Sumida CDRH5D18-220 Coilcraft DO1608C-223	0.38 (max) 0.28 (max) 0.32 (typ)	680 760 700
47	Sumida CD43-470 Coilcraft DO1608C-473	0.84 (max) 0.56 (typ)	440 500
100	Sumida CD54-101 Coilcraft DO1608C-104	0.7 (max) 1.1(typ)	520 310

Table 1. Surface-Mount Inductor Information

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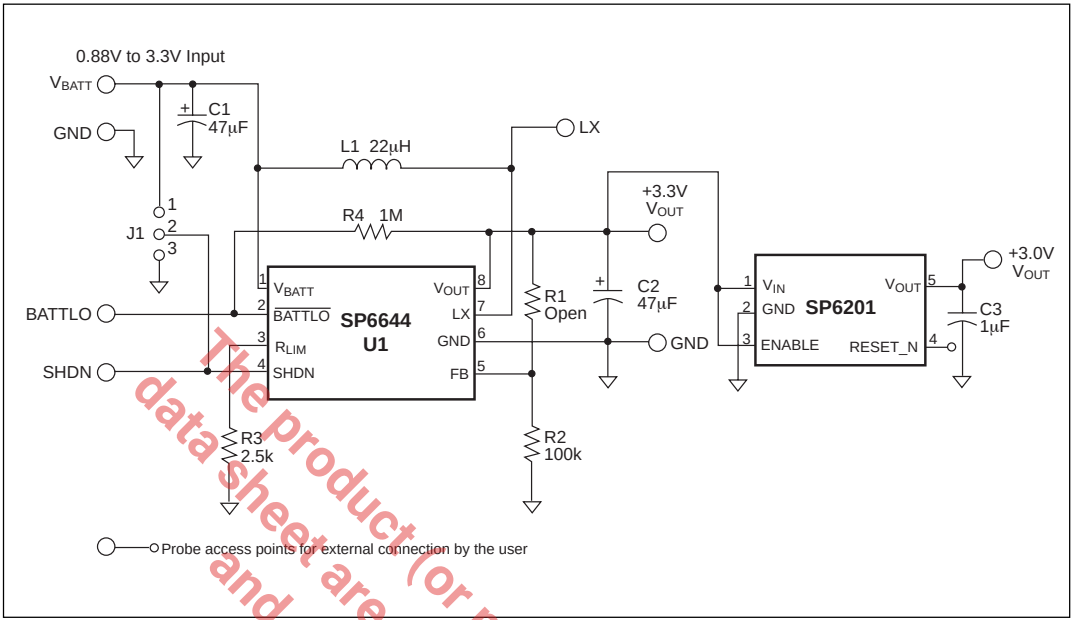
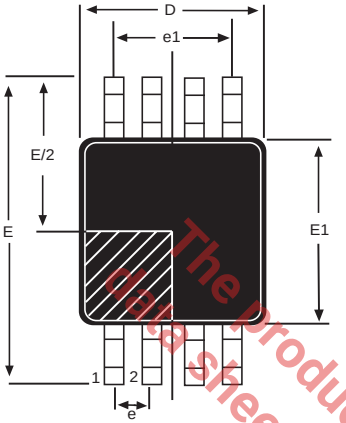


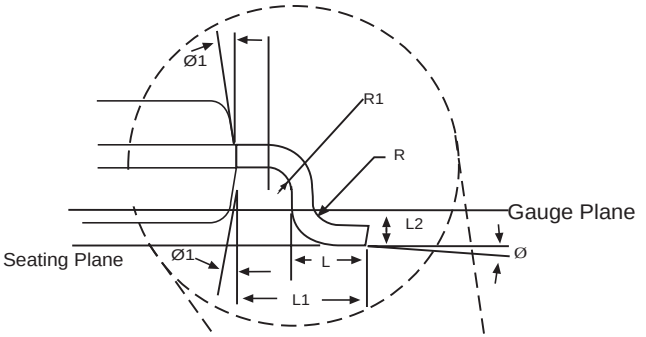
Figure 29. Schematic SP6644/6201 DC/DC LDO Combination

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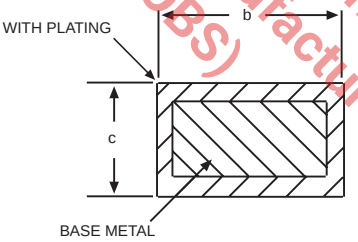


Pin #1 indentifier must be indicated within this shaded area (D/2 * E1/2)









Section B-B

8 Pin MSOP JEDEC MO-187 (AA) Variation			
SYMBOL	MIN	NOM	MAX
A	-	-	1.1
A1	0	-	0.15
A2	0.75	0.85	0.95
b	0.22	-	0.38
c	0.08	-	0.23
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
e		0.65 BSC	
e1		1.95 BSC	
L	0.4	0.6	0.8
L1		0.95 REF	
L2		0.25 BSC	
N	-	8	-
R	0.07	-	-
R1	0.07	-	-
ø	0º	-	8º
ø1	0º	-	15º

Note: Dimensions in (mm)

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ORDERING INFORMATION

Part Number	Temperature Range	Package Type
SP6644EU	-40°C to +85°C	8-Pin MSOP
SP6644EU/TR	-40°C to +85°C	8-Pin MSOP
SP6645EU	-40°C to +85°C	8-Pin MSOP
SP6645EU/TR	-40°C to +85°C	8-Pin MSOP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6644EU/TR = standard; SP6644EU-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2500 for MSOP.

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